USB PD MCU CH543, USB MCU CH541

Datasheet

Version: 1E

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1. Overview

CH543 is a USB and USB PD enhanced E8051 core MCU compatible with MCS51 instruction set. 79% of its instructions are single-byte single-cycle instructions, and the average instruction speed is 8 to 15 times faster than that of the standard MCS51.

CH543 has built-in 16K Flash-ROM, 256-byte internal iRAM and 256-byte on-chip xRAM. xRAM supports direct memory access (DMA).

CH543 provides a built-in USB Power Delivery controller and PD BMC PHY transceiver. CH543 supports USB type C, BC, PD2.0, and PD3.0, and supports 12V high-voltage power. It can act as PMIC used for power management, Sink, Source and DRP.

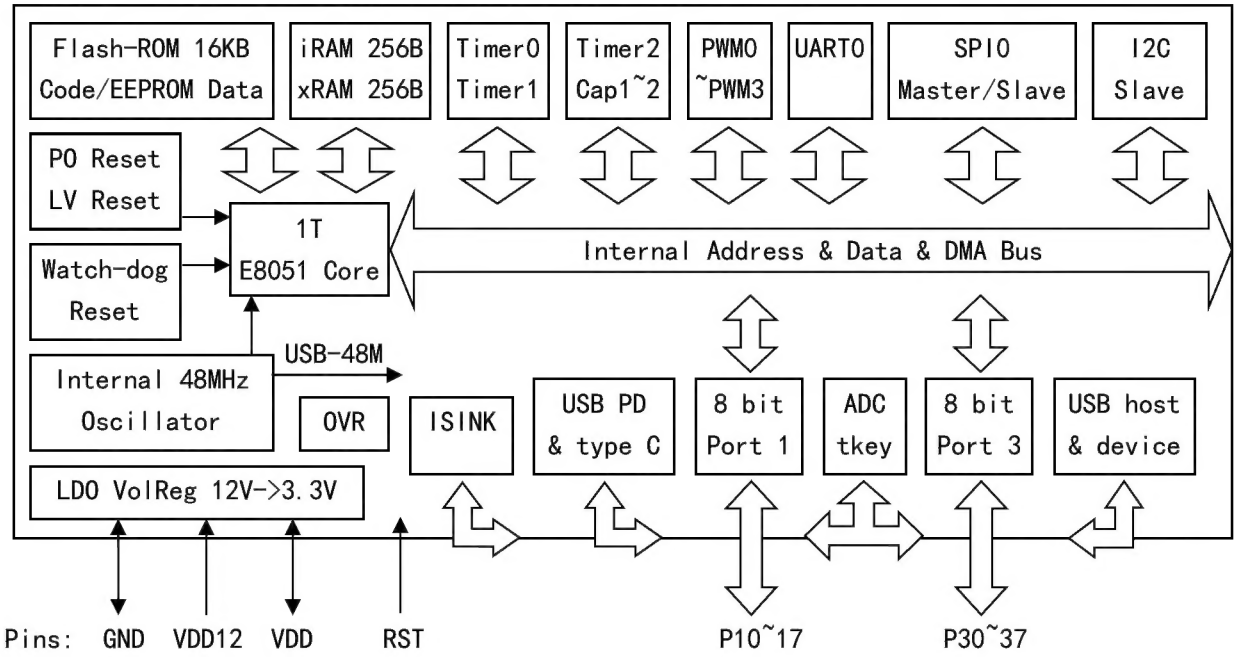
CH543 provides a built-in USB host controller and transceiver, and supports full-speed and low-speed USB Host and USB Device.

CH543 also has built-in 12-bit ADC, capacitive touch key detection module, built-in clock, 3 sets of timers and 2 signal capture, 4-channel PWM, asynchronous serial port, SPI, I2C slave, programmable current filling module and other functional modules.

The CH541 is a USB microcontroller supporting 12V power supply. The CH541 is based on the CH543 with the USB PD, USB host, and programmable fill current modules removed and the type C module retained, otherwise it is the same as the CH543, refer to the CH543 manual and literature.

<table>
<tr><th>Model</th><th>Program + Boot + EEPROM</th><th>xRAM iRAM</th><th>USB Master/ slave</th><th>USB PD type C</th><th>Timer/ Capture</th><th>UART</th><th>General PWM</th><th>I2C slave</th><th>SPI Master/ slave</th><th>Programmable sink current</th><th>12-bit ADC</th><th>Capacitive touchkey</th></tr>
<tr><td>CH543</td><td rowspan="2">14KB+2KB can be combined for all user programs</td><td rowspan="2">256 +256</td><td>Master/ slave</td><td>√</td><td rowspan="2">3 timers/ 2-channel capture</td><td rowspan="2">√</td><td rowspan="2">4-channel</td><td rowspan="2">√</td><td rowspan="2">√</td><td>512 level</td><td rowspan="2">12-channel</td><td rowspan="2">11-channel</td></tr>
<tr><td>CH541</td><td>Device</td><td>Only type C</td><td>None</td></tr>
</table>

The following is the internal block diagram of CH543 for reference only.



2. Features

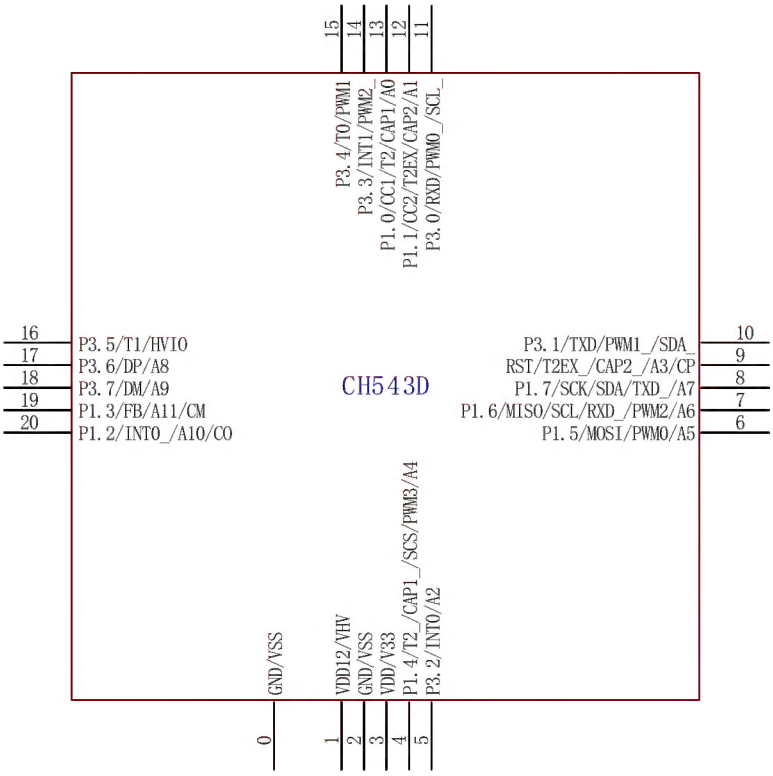
- Core: Enhanced E8051 core, compatible with MCS51 instruction set, 79% of instructions are single-byte single-cycle instructions, and the average command speed is 8 to 15 times faster than that of the standard MCS51. Special XRAM data fast copy instruction, and double DPTR pointers.
- ROM: 16KB nonvolatile memory Flash-ROM which supoorts 10K times of erase/write operations. All can be used for the program address space. Or it can be divided into a 14KB program address space, a 256B data address space EEPROM and a 1.75KB BootLoader/ISP program space.
- EEPROM: 256-byte data address space EEPROM. It is divided into 4 independent blocks, and supports single-byte read, single-byte write, block write (1 ~ 64 bytes), block erase (64 bytes) operations. In a typical environment, generally it supports 100K times of erase/write operations.
- OTP: One time programmable data storage area (OTP) has a total of 32 bytes, and supports double-byte read (4 bytes) and single byte write.
- RAM: 256-byte internal iRAM can be used for fast temporary storage of data and stack. 256-byte on-chip xRAM can be used for data temporary storage and DMA to USBor USB PD.
- USB: USB controller and USB transceiver support USB-Host mode USB-Device mode, and support USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps). Support data packet of up to 64 bytes. Built-in FIFO. Support DMA. USB ports support BC charging protocols. Support UART RXD/TXD pin mapping.
- USB PD and type C: USB Power Delivery controller and PD transceiver PHY. Support USB type-C host/device detection, auto BMC encoder/decoder and CRC, and hardware edge control. DMA capability. USB PD2.0 and PD3.0 power delivery control. DRP.
- Timer: 3 16-bit timers (T0, T1 and T2) are standard MCS51 timers.
- Capture: The T2 timer is extended to support 2-channel signal capture. Leading edge trigger, trailing edge trigger, and periodic detection.
- PWM: 4-channel 8-bit ordinary PWM outputs, or 2-channel high-precision 12-bit PWM outputs. Support interleaved output.
- UART: Standard MCS51 UART. Support up to 3 Mbps or 460800 bps baud rate.
- SPI: Master/Slave mode. Built-in FIFO. The clock can be up to around half of the system clock frequency. Serial data input/output simplex multiplex.
- I2CS: I2C slave controller supports 1 MHz clock.
- ISINK: 512 levels of programmable sink current, equivalent to 9-bit DAC, supports PPS.
- ADC: 12-channel 12-bit A/D converter. Optionally, input buffering or simple amplification.
- Touch-Key: 11-channel capacitive touch-key detection. Each ADC channel except RST supports touch-key detection.
- GPIO: Up to 17 GPIO pins (USB, USB PD and RST pins are included). Support MCS51 compatible quasi-bidirectional mode, newly added high inpendance input mode, push-pull output mode and open-drain output mode.
- P3.5 supports VDD12 high-voltage 12V input/output. The RST pin support VDD12 high-voltage 12V as a general-purpose input.
- Interrupt: 14 interrupt signal sources, including 6 interrupts compatible with standard MCS51 (INT0, T0, INT1, T1, UART0 and T2), and 8 extended interrupts (SPI0, I2C, USB, ADC, USB PD, PWMX/CMP, GPIO and WDOG). The GPIO interrupt can be selected from several pins.
- Watch-Dog: 8-bit presettable watchdog timer (WDOG), supports timing interrupt.
- Reset: 7 reset signal sources. Built-in power-on reset module (POR), low voltage detection reset module (LVR) and supply over-voltage reset module (OVR). Support software reset and watchdog

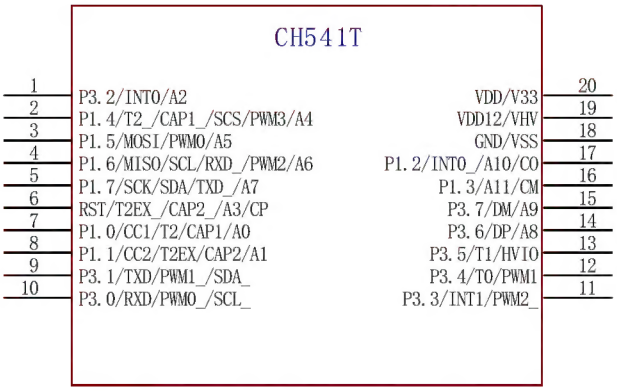
overflow reset. Optional pins for external input reset. Optional USB PD hardware reset.

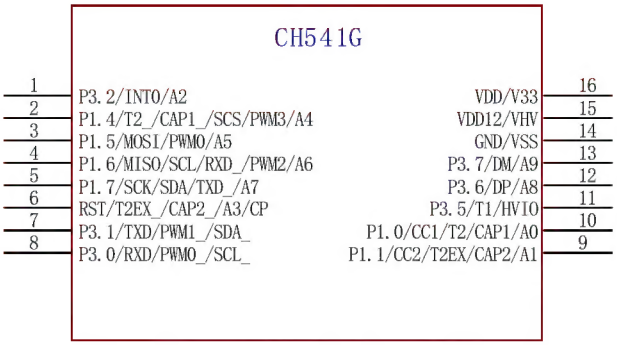
- Clock: Built-in 48 MHz clock source, used to generate system clock frequency (Fsys) and USB clock as required.
- Power: Built-in 12V to 3.3V or 4.7V low dropout regulator, used for USB, I/O, ADC and so on. VDD12 supports 5V/3.3V/9V or even 12V/2.8V supply voltage.
- Supports VDD12 high-voltage discharge, and supports the RST pin 12V high-voltage discharge.
- Sleep: Low-power sleep. Supports wake up USB, USB PD/type C, UART0, SPI0 and part of GPIOs externally.
- Built-in unique ID. Supports ID number and calibration.
- Available in small QFN, low cost SOP16 and other package formats.

3. Package

Package Form	Shaping Width		Pin Spacing		Package Description	Order model
QFN-20	3*3mm		0.40mm	15.7mil	Quad Flat No-Lead Package	CH543D
TSSOP-20	4.4mm	173mil	0.65mm	25mil	Thin Shrink Small Outline Package	CH541T
SOP-16	3.9mm	150mil	1.27mm	50mil	Small Outline Package	CH541G







4. Pin Definitions

Pin No.			Pin name	Other function names (Left function with the highest priority)	Description
543D	541T	541G			
1	19	15	VDD12	VHV	External power input of the voltage regulator (LDO), and high-voltage I/O power input of P3.5. An external decoupling capacitor is required.
3	20	16	VDD	V33/VIO	Internal voltage regulator (LDO) output, USB power and I/O power input. When supply voltage is less than 3.6V, connect to VDD12 to input external power. When supply voltage is greater than 3.6V, connect to an external decoupling capacitor.

0,2	18	14	GND	VSS	Ground. Exposed-Pad 0# pin is EPAD.
13	7	9	P1.0	CC1/T2/CAP1/A0	A0~A11: 12 channels of ADC analog signal inputs, AIN0~AIN11. A0~A2, A4～A11: 11 channels of touch-key inputs. T2: External count input / clock output of timer/counter 2. T2EX: Reload/ capture input of timer/counter 2. CAP1, CAP2: Capture input 1, 2 of timer/counter 2. SCS, MOSI, MISO, SCK: SPI0 interfaces. SCS is chip select input. MOSI is master output / slave input. MISO is master input / slave output. SCK is serial clock master output / slave input. CC1, CC2: CC signal-ends of USB PD/type C. Default to be pulled down. FB: Current draw side of the programmable sink current ISINK. PWM0~PWM3: 4 channels of PWM outputs. SCL, SDA: I2C slave serial clock input, bidirectional serial data. CP, CM, CO: Positive input, negative input and output of CM. RXD, TXD: UART0 serial data input, serial data output. INT0, INT1: External interrupt 0 input, external interrupt 1 input. T0, T1: Timer 0 external input, timer 1 external input. DM, DP: D-, D+ signals of USB host or USB device. HVIO: High-voltage GPIO with VDD12 as I/O power. RST: External reset input. Active high. Built-in pull-down resistor. INT0_, T2_/CAP1_, T2EX_/CAP2_, RXD_, TXD_: INT0/T2/CAP1/T2EX/CAP2/RXD/TXD pin mapping. RXD10_/TXD10_, RXD11_/TXD11_: RXD/TXD pin mapping when MASK_UART_I2C is under option 10 and option 11.
12	8	8	P1.1	CC2/T2EX/CAP2/A1	
20	17	None	P1.2	INT0_/A10/CO	
19	16	None	P1.3	FB/A11/CM	
4	2	2	P1.4	T2_/CAP1_/SCS /PWM3/A4	
6	3	3	P1.5	MOSI/PWM0/A5	
7	4	4	P1.6	MISO/SCL/RXD_ /PWM2/A6	
8	5	5	P1.7	SCK/SDA/TXD_ /A7	
11	10	8	P3.0	RXD/PWM0_/SCL _	
10	9	7	P3.1	TXD/PWM1_/SDA _	
5	1	1	P3.2	INT0/A2	
14	11	None	P3.3	INT1/PWM2_	
15	12	None	P3.4	T0/PWM1	
16	13	11	P3.5	T1/HVIO	
17	14	12	P3.6	DP/TXD11_ /RXD10_/A8	
18	15	13	P3.7	DM/TXD10_ /RXD11_/A9	
9	6	6	RST	T2EX_/CAP2_/A3 /CP	

Note: Please refer to this table for other packages. The functions of pins with the same name are the same. After reset, P1.0/P1.1 defaults to be pulled down 5.1K. P1.2/P1.3 defaults to be floating. P3.6/P3.7 defaults to be weak pulled down 2uA. RST defaults to be pulled down 40K. P1.7 on CH543 defaults to be weak pulled up 5uA. Other GPIOs and P1.7 on CH541 default to be pulled up compatible with MCS51. The USB transceiver is designed based on USB2.0 fully built-in. P3.6/P3.7 cannot be connected in series with resistors when used for USB.

5. Special function register (SFR)

The following abbreviations may be used in this datasheet to describe the registers:

Abbreviation	Description
RO	Software can only read these bits.
WO	Software can only write to this bit. The read value is invalid.
RW	Software can read and write to these bits.
H	End with it to indicate a hexadecimal number
B	End with it to indicate a binary number

5.1 SFR Introduction and Address Distribution

CH543 controls and manages the device, and sets the operating mode via the special function registers (SFR).

SFRs occupy 80h to FFh addresses of the internal data address space and can only be accessed by direct address commands. Registers with the x0h/x8h addresses can be accessed by bits to avoid modifying the values of other bits when accessing a specific bit. Other registers with the addresses that are not the multiple of 8 can only be accessed by bytes.

Some SFRs can only be written in safe mode, while they are read-only in non-safe mode , such as GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL, POWER_CFG, GPIO_IE, ISINK_DATA.

Some SFRs have one or more aliases, such as SPI0_CK_SE/SPI0_S_PRE, UDEV_CTRL/UHOST_CTRL, UEP1_CTRL/UH_SETUP, UEP2_CTRL/UH_RX_CTRL, UEP2_T_LEN/UH_EP_PID, UEP3_CTRL/UH_TX_CTRL, UEP3_T_LEN/UH_TX_LEN, UEP2_3_MOD/UH_EP_MOD, UEP2_DMA_L/UH_RX_DMA_L, UEP3_DMA_L/UH_TX_DMA_L, ROM_ADDR_L/ROM_DATA_LL, ROM_ADDR_H/ROM_DATA_LH, ROM_DATA_HL/ROM_DAT_BUF, ROM_DATA_HH/ROM_BUF_MOD.

Some addresses correspond to several independent SFRs, such as: SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

CH543 contains all 8051 standard SFR registers, and other device control registers are added. See the table below for the specific SFRs.

Table 5.1.1 Table of internal special function registers (SFR)

SFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP			WDOG_COUNT
0xF0	B	ANA_CTRL	TKEY_CTRL	ADC_CTRL	ADC_DAT_L	ADC_DAT_H	ADC_CHAN	
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD UH_EP_MOD	UEP0_DMA_L		UEP1_DMA_L	
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L UH_RX_DMA_L		UEP3_DMA_L UH_TX_DMA_L	
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN		
0xD0	PSW	UDEV_CTRL UHOST_CTRL	UEP1_CTRL UH_SETUP	UEP1_T_LEN	UEP2_CTRL UH_RX_CTRL	UEP2_T_LEN UH_EP_PID	UEP3_CTRL UH_TX_CTRL	UEP3_T_LEN UH_TX_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	UPD_INT_FG	UPD_INT_EN	UPD_CTRL	UPD_DATA	UPD_DMA_L		CC1_CTRL	CC2_CTRL

0xB8	IP	CLOCK_CFG	POWER_CFG	UPD_TIMER	UPD_COUNT	UPD_T_LEN	UPD_T_SOP	UPD_CRC32
0xB0	P3	GLOBAL_CFG	GPIO_IE	PIN_RST	USB_PULL		PWM_CYCLE_L	PWM_CYCLE_H
0xA8	IE	WAKE_CTRL	PIN_FUNC				ISINK_DATA	ISINK_LSB
0xA0	I2CS_STAT	SAFE_MOD CHIP_ID	XBUS_AUX	PWM_DATA3	I2CS_CTRL	I2CS_DEV_A	I2CS_ADDR	I2CS_DATA
0x98	SCON	SBUF	PWM_DATA2	PWM_DATA1	PWM_DATA0	PWM_CTRL	PWM_CK_SE	PWM_CTRL2
0x90	P1	PIN_MISC	P1_MOD_OC	P1_DIR_PU	P1_ANA_PIN	P3_ANA_PIN	P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_HL ROM_DAT_BUF	ROM_DATA_HH ROM_BUF_MOD
0x80		SP	DPL	DPH	ROM_ADDR_L ROM_DATA_LL	ROM_ADDR_H ROM_DATA_LH	ROM_CTRL ROM_STATUS	PCON

Notes: (1) Registers in red text can be accessed by bits.

(2). The following table shows the description of the color boxes.

	Register address
	SPI0 registers
	I2C registers
	ADC, TouchKey, CMP registers
	USB registers
	Timer/counter 2 registers
	Port setting registers
	PWMX registers
	USB PD, USB type C registers
	Timer/counter 0 and 1 registers
	UART0 registers
	ISINK registers
	Flash-ROM registers

5.2 SFR Classification and Reset Value

Table 5.2 Description and reset value SFRs

Function Classification	Name	Address	Description	Reset value
System setting registers	B	F0h	B register	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	PSW	D0h	Program status word register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (CH543 boot loader)	1110 0000b
			Global configuration register (CH543 application program)	1100 0000b
			Global configuration register (CH541 boot loader)	0110 0000b

			Global configuration register (CH541 application program)	0100 0000b
	CHIP_ID	A1h	CH543 ID (read only)	0100 0011b
			CH541 ID (read only)	0100 0001b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b
	DPH	83h	Data address pointer high 8 bits	0000 0000b
	DPL	82h	Data address pointer low 8 bits	0000 0000b
	DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power control registers	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	POWER_CFG	BAh	Power management configuration register	0000 0xxxb
	CLOCK_CFG	B9h	System clock configuration register	0000 0011b
	WAKE_CTRL	A9h	Wakeup control register	0000 0000b
	PCON	87h	Power control register (in power on reset state)	0001 0000b
Interrupt control registers	IP_EX	E9h	Extend interrupt priority control register	0000 0000b
	IE_EX	E8h	Extend interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
	GPIO_IE	B2h	GPIO interrupt enable register	0000 0000b
Flash-ROM registers	ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HI	8Eh	ROM_DATA_HL and ROM_DATA_HH constitute a 16-bit SFR	xxxxh
	ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase and write operation	xxxx xxxxb
	ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase and write operation	xxxx xxxxb
	ROM_STATUS	86h	flash-ROM status register (read only)	0000 0000b
	ROM_CTRL	86h	flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h	flash-ROM address register high byte	xxxx xxxxb
	ROM_ADDR_L	84h	flash-ROM address register low byte	xxxx xxxxb
	ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh
	ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LO	84h	ROM_DATA_LL and ROM_DATA_LH constitute a 16-bit SFR	xxxxh
Port setting	PIN_RST	B3h	RST pin configuration register	0000 0111b

registers	PIN_FUNC	AAh	Pin function selection register	0000 0000b
	XBUS_AUX	A2h	External bus auxiliary setting register	0000 0000b
	P3_DIR_PU	97h	P3 port direction control and pull-up enable register	1111 1111b
	P3_MOD_OC	96h	P3 port output mode register	1111 1111b
	P3_ANA_PIN	95h	P3 port analog mode control register	0000 0000b
	P1_DIR_PU	93h	CH543: P1 port direction control and pull-up enable register	0111 0000b
			CH541: P1 port direction control and pull-up enable register	1111 0000b
	P1_MOD_OC	92h	P1 port output mode register	1111 1111b
	P1_ANA_PIN	94h	P1 port analog mode control register	0000 0000b
	PIN_MISC	91h	CH543: Miscellaneous I/O control register	1000 0000b
			CH541: Miscellaneous I/O control register	0000 0000b
	P3	B0h	P3 port input/output register	1111 1111b
	P1	90h	P1 port input/output register	1111 1111b
Timer/counter 0 and 1 registers	TH1	8Dh	Timer1 count high byte	0000 0000b
	TH0	8Ch	Timer0 count high byte	0000 0000b
	TL1	8Bh	Timer1 count low byte	0000 0000b
	TL0	8Ah	Timer0 count low byte	0000 0000b
	TMOD	89h	Timer0/1 mode register	0000 0000b
	TCON	88h	Timer0/1 control register	0000 0000b
UART0 registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timer/counter 2 registers	T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	0000 0000b
	T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	0000 0000b
	T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	0000h
	TH2	CDh	Timer2 count high byte	0000 0000b
	TL2	CCh	Timer2 count low byte	0000 0000b
	T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
	RCAP2H	CBh	Count reload/capture 2 data register high byte	0000 0000b
	RCAP2L	CAh	Count reload/capture 2 data register low byte	0000 0000b
	RCAP2	CAh	RCAP2L and RCAP2H constitute a 16-bit SFR	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
PWMX registers	PWM_CYCLE_H	B7h	PWM cycle register high byte	0000 0000b
	PWM_CYCLE_L	B6h	PWM cycle register low byte	0000 0000b
	PWM_CYCLE	B6h	PWM_CYCLE_L and PWM_CYCLE_H constitute a 16-bit SFR	0000h

	PWM_DATA3	A3h	PWM3 data register	0000 0000b
	PWM_CTRL2	9Fh	PWM extend control register	0000 0000b
	PWM_CK_SE	9Eh	PWM clock setting register	0000 0000b
	PWM_CTRL	9Dh	PWM control register	0000 0010b
	PWM_DATA0	9Ch	PWM0 data register	0000 0000b
	PWM_DATA1	9Bh	PWM1 data register	0000 0000b
	PWM_DATA2	9Ah	PWM2 data register	0000 0000b
SPI0 registers	SPI0_SETUP	FCh	SPI0 setup register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data receive/transmit register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 status register	0000 1000b
I2C slave registers	I2CS_DATA	A7h	I2CS slave data receive/transmit register	xxxx xxxxb
	I2CS_ADDR	A6h	I2CS slave data address register (read only)	xxxx xxxxb
	I2CS_DEV_A	A5h	I2CS slave device address register	0000 0000b
	I2CS_CTRL	A4h	I2CS slave control register	0000 0x00b
	I2CS_STAT	A0h	I2CS slave status register	0000 1100b
ADC /TKEY /CMP registers	ADC_CHAN	F6h	ADC analog signal channel selection register	0000 0000b
	ADC_DAT_H	F5h	ADC result data high byte (read only)	0000 xxxxb
	ADC_DAT_L	F4h	ADC result data low byte (read only)	xxxx xxxxb
	ADC_DAT	F4h	ADC_DAT_L and ADC_DAT_H constitute a 16-bit SFR	0xxxh
	ADC_CTRL	F3h	ADC control and status register	0000 0000b
	TKEY_CTRL	F2h	Touch-key charge impulse width control register (write only)	0000 0000b
	ANA_CTRL	F1h	Analog CMP control register	0000 0000b
ISINK registers	ISINK_LSB	AFh	Programmable sink current ISINK preset lowest bit register (write only)	0000 0000b
	ISINK_LSB	AFh	Programmable sink current ISINK current lowest bit register (read only)	0000 0000b
	ISINK_DATA	AEh	Programmable sink current ISINK high 8-bit data register	0000 0000b
USB registers	UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
	UEP0_DMA_L	ECh	Endpoint 0 buffer start address low byte	xxxx xxxxb
	UEP2_3_MOD	EBh	Endpoint 2, 3 mode control register	0000 0000b
	UH_EP_MOD	EBh	USB host endpoint mode control register	0000 0000b
	UEP4_1_MOD	EAh	Endpoint 1 mode control register	0000 0000b
	UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	xxxx xxxxb
	UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb

	UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
	UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint 0 transmission length register	0000 0000b
	UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
	USB_RX_LEN	DBh	USB reception length register (read only)	0xxx xxxxb
	USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read only)	0011 xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0000 0000b
	UEP3_T_LEN	D7h	Endpoint 3 transmission length register	0000 0000b
	UH_TX_LEN	D7h	USB host transmission length register	0000 0000b
	UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
	UH_TX_CTRL	D6h	USB host transmission endpoint control register	0000 0000b
	UEP2_T_LEN	D5h	Endpoint 2 transmission length register	0000 0000b
	UH_EP_PID	D5h	USB host token setting register	0000 0000b
	UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
	UH_RX_CTRL	D4h	USB host reception endpoint control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint 1 transmission length register	0000 0000b
	UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
	UH_SETUP	D2h	USB host auxiliary setup register	0000 0000b
	UDEV_CTRL	D1h	USB device port control register	0000 0000b
	UHOST_CTRL	D1h	USB host port control register	0000 0000b
	USB_PULL	B4h	USB port pull-up/pull-down resistance/current control register	0001 0001b
USB PD /type C registers	CC2_CTRL	C7h	PD/type C CC2 control register	0000 0011b
	CC1_CTRL	C6h	PD/type C CC1 control register	0000 0011b
	UPD_DMA_L	C4h	PD buffer start address low byte	xxxx xxxxb
	UPD_DATA	C3h	PD data register	xxxx xxxxb
	UPD_CTRL	C2h	PD control register	0000 0010b
	UPD_INT_EN	C1h	PD interrupt enable register	0000 0000b
	UPD_INT_FG	C0h	PD interrupt flag register	0000 0000b
	UPD_CRC32	BFh	PD CRC32 data check register (read only)	xxxx xxxxb
	UPD_T_SOP	BEh	PD transmit SOP configuration register	0000 0000b
	UPD_T_LEN	BDh	PD transmission length register	0000 0000b
	UPD_COUNT	BCh	PD data byte count register (read only)	0xxx xxxxb
	UPD_TIMER	BBh	PD BMC timer register	0000 0000b

5.3 General-purpose 8051 Register

Table 5.3.1 General-purpose 8051 registers

Name	Address	Description	Reset value
B	F0h	B register	00h
A、ACC	E0h	Accumulator	00h
PSW	D0h	Program status word register	00h
GLOBAL_CFG	B1h	Global configuration register (CH543 boot loader)	E0h
		Global configuration register (CH543 application program)	C0h
		Global configuration register (CH541 boot loader)	60h
		Global configuration register (CH541 application program)	40h
CHIP_ID	A1h	CH543 ID (read only)	43h
		CH541 ID (read only)	41h
SAFE_MOD	A1h	Safe mode control register (write only)	00h
PCON	87h	Power control register (in power on reset state)	10h
DPH	83h	Data address pointer high 8 bits	00h
DPL	82h	Data address pointer low 8 bits	00h
DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
SP	81h	Stack pointer	07h

B register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic operation register, mainly used for multiplication and division operations, can be accessed by bits.	00h

A accumulator (A、ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic operation accumulator, can be accessed by bits.	00h

Program status word register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry flag bit: used to record the carry or borrow of the highest bit when performing arithmetic operations and logical operations. In 8-bit addition operation, for the carry of the highest bit, this bit is set, otherwise it is cleared. In 8-bit subtraction operation, for the borrow, this bit is set, otherwise it is cleared. The logical command can set and clear this bit.	0
6	AC	RW	Auxiliary carry flag bit. In addition and subtraction operations, for the carry or borrow from the lower 4 bits to the higher 4 bits, AC is set, otherwise it is cleared.	0
5	F0	RW	General flag bit 0, can be accessed by bits. User-defined.	0

			Cleared and set by software.	
4	RS1	RW	High bit of register bank selection bit	0
3	RS0	RW	Low bit of register bank selection bit	0
2	OV	RW	Overflow flag bit. In addition and subtraction operations, if the operation result exceeds 8-bit binary number, OV is set to 1 and the flag overflows, otherwise it is cleared.	0
1	F1	RW	General flag bit 1, can be accessed by bits. User-defined. Cleared and set by software.	0
0	P	RO	Parity flag bit. This bit records the parity of '1' in accumulator A after the command is executed. If the number of '1' is an odd number, P is set. If the number of '1' is an even number, P is cleared.	0

The state of processor is stored in the program status word register (PSW), and PSW can be accessed by bits. The status word includes the carry flag bit, auxiliary carry flag bit for BCD code processing, parity flag bit, overflow flag bit, as well as RS0 and RS1 for working register bank selection.The area where the working register bank is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 working register bank selection table

RS1	RS0	Working register bank
0	0	Bank 0 (00h-07h)
0	1	Bank 1 (08h-0Fh)
1	0	Bank 2 (10h-17h)
1	1	Bank 3 (18h-1Fh)

Table 5.3.3 Operations affecting flag bits (X indicates that the flag bit is related to the operation result)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data address pointer (DPTR):

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH constitute a 16-bit data pointer (DPTR), which is used to access xRAM data memory and program memory. Actually, the DPTR corresponds to 2 sets of physical 16-bit data pointers (DPTR0 and

DPTR1), which are dynamically selected by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer. Mainly used for program calls and interrupt calls as well as data in/out of the stack	07h

Specific functions of stack: protect breakpoint and protect site, and carry out management on the first-in last-out principle. During instack, SP pointer automatically adds 1, to save the data/breakpoint information. During outstack, SP pointer points to the data unit and automatically substracts 1. The initial value of SP is 07h after reset, and the corresponding default stack storage starts from 08h.

5.4 Special Register

Global configuration register (GLOBAL_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Always 11 for CH543.	11b
			Always 01 for CH541.	01b
5	bBOOT_LOAD	RO	Boot loader status bit, used to distinguish ISP boot loader or application program. Set to 1 during power on, and cleared during software reset. For the chip with ISP boot loader, if this bit is 1, it has never been reset by software and it is usually in ISP boot loader running after power on state. If this bit is 0, it has been reset by software, and it is usually in application state.	1
4	bSW_RESET	RW	Software reset control bit. If it is set to 1, software reset occurs. Automatically reset by hardware.	0
3	bCODE_WE	RW	Flash-ROM write enable bit Write protection if this bit is 0. Flash-ROM can be written and erased if this bit is 1	0
2	bDATA_WE	RW	Flash-ROM DataFlash area write enable bit Write protection if this bit is 0. DataFlash area can be written and erased if this bit is 1.	0
1	Reserved	RO	Reserved	0
0	bWDOG_EN	RW	Watchdog reset enable bit If this bit is 0, watchdog is only used as a timer. If this bit is 1, watchdog reset enabled when timing overflows.	0

Chip ID (CHIP_ID):

Bit	Name	Access	Description	Reset value
[7:0]	CHIP_ID	RO	Always 43h for CH543. Used to identify the chip.	43h
			Always 41h for CH541. Used to identify the chip.	41h

Safe mode control register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	Used to enter and terminate safe mode	00h

Some SFRs can only be written in safe mode, while they are always read-only in non-safe mode. Steps for entering safe mode:

(1). Write 55h into this register.

(2). And then write AAh into this register.

(3). After that, they are in safe mode for about 13 to 23 system clock cycles, and one or more safe class SFR or ordinary SFR can be rewritten in such validity period.

(4). Automatically terminate the safe mode after the expiration of the above validity period.

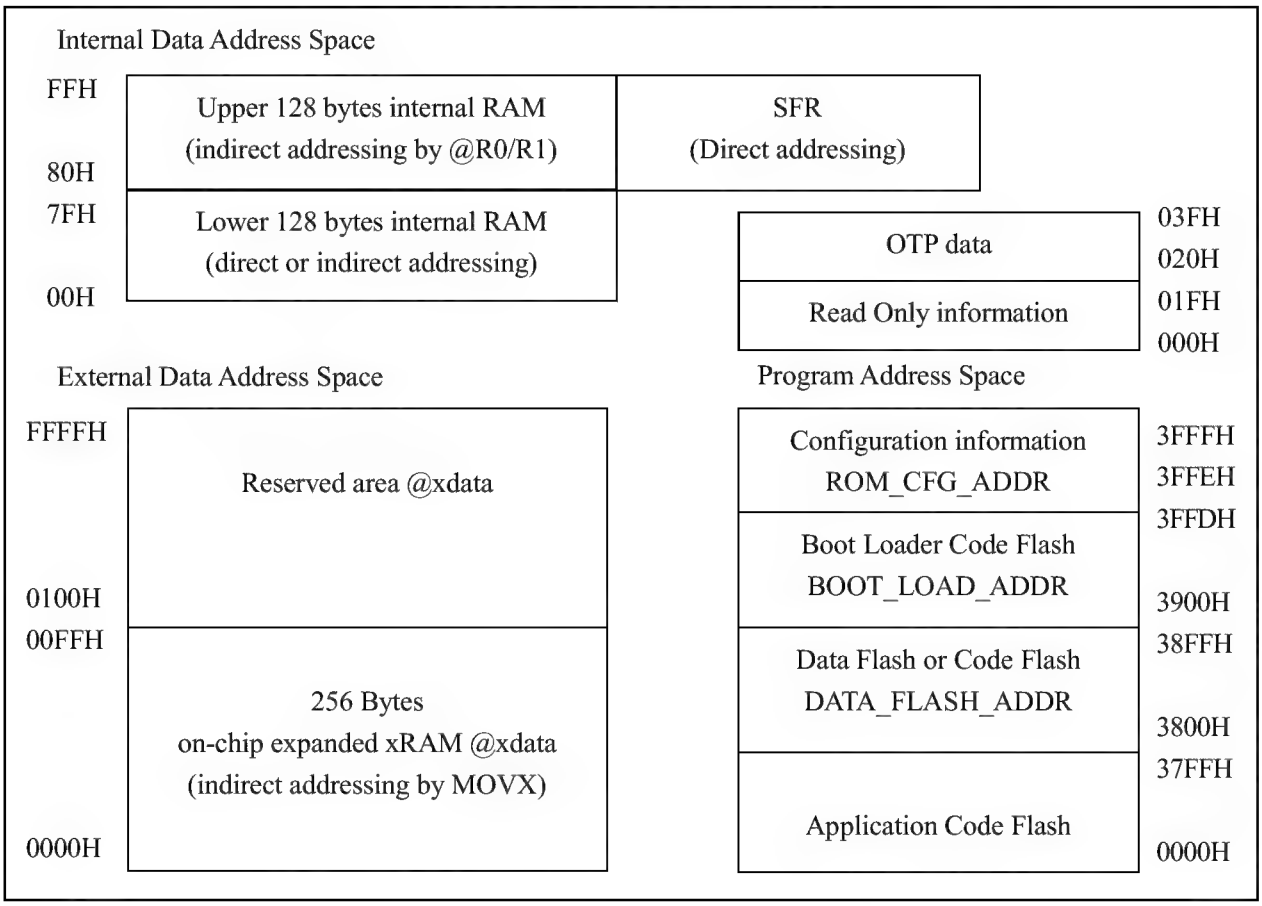
(5). Alternatively, write any value to the register to prematurely terminate safe mode.

6. Memory Structure

6.1 Memory Space

CH543 addressing space is divided into program address space, internal data address space, external data address space, read only information and OTP data space.

Figure 6.1 Memory structure diagram



6.2 Program Address Space

The program address space is 64KB in total, of which the lower 16KB provides flash-ROM, as shown in Figure 6.1, which consists of the Code Flash area to save the command code, the Data Flash area to save the nonvolatile data, and the Configuration Information area to configure the information.

Data Flash (EEPROM) address ranges from 3800h to 38FFH, and supports single byte read (8 bits), single byte write (8 bits), block write (1 ~ 64 bytes), and block erase (64 bytes) operations. The data remains unchanged after power down, and it can also be used as Code Flash.

Code Flash includes the application code for the low address area and the boot loader code for the high address area, or these two areas and Data Flash may be combined to save a single application code.

Configuration information area has 16 bits of data, which is set by the programmer as required, refer to Table 6-1.

Table 6.2 flash-ROM configuration information description

Bit address	Bit name	Description	Recommended value

15	Code_Protect	flash-ROM code and data protection mode: 0: Read enabled. 1: Disable the programmer to read out, and keep the program secret.	0/1
14	No_Boot_Load	Enable BootLoader startup mode: 0: Startup from the application from 0000h address. 1: Startup from the boot loader from 3900h address.	1
13	En_Long_Reset	Enable extra delay reset during power on reset: 0: Standard short reset. 1: Wide reset, with extra 44mS reset time added	0
12	En_RST_RESET	Enable RST as manual reset input pin: 0: Disabled. 1: RST enabled.	0
11		Reserved	0
10		Reserved	0
9	Must_1	(Automatically set to 1 by the programmer as required)	1
8	Must_0	(Automatically set to 0 by the programmer as required)	0
[7:3]	All_0	(Automatically set to 00000b by the programmer as required)	00000b
[2]	LDO_VOL	Select output voltage of the LDO internal voltage regulator (I/O voltage): 0: 3.3V selected. 1: 4.7V selected.	0
[1]	Default_0	(Automatically set to 0 by the programmer as required)	0
[0]	LV_RST_VOL (Vpot)	Select threshold of the LVR module (8% error): 0: 2.8V selected. 1: 2.3V selected.	0

6.3 Data Address Space

The internal data address space which occupies 256 bytes, as shown in Figure 6.1, has been all used for SFR and iRAM. iRAM is used for stack and fast temporary data storage, and can be subdivided into the working registers (R0-R7), bit variable (bdata), byte variable (data) and idata, etc.

The external data address space occupies 64KB, as shown in Figure 6.1. Except that the lower 256 bytes are used for on-chip expanded xRAM, the remaining 0100h to FFFFh addresses are reserved.

Read-only information area and OTP data area each has 32 bytes, as shown in Figure 6.1, and they need to be accessed through a dedicated operation.

6.4 Flash-ROM Register

Table 6.4 flash-ROM operation registers

Name	Address	Description	Reset value
ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxh

ROM_DATA_HI	8Eh	ROM_DATA_HL and ROM_DATA_HH constitute a 16-bit SFR	xxxxh
ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxh
ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxh
ROM_STATUS	86h	flash-ROM status register (read only)	00h
ROM_CTRL	86h	flash-ROM control register (write only)	00h
ROM_ADDR_H	85h	flash-ROM address register high byte	xxh
ROM_ADDR_L	84h	flash-ROM address register low byte	xxh
ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh
ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LO	84h	ROM_DATA_LL and ROM_DATA_LH constitute a 16-bit SFR	xxxxh

flash-ROM address resigter (ROM_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_ADDR_H	RW	flash-ROM address high byte	xxh
[7:0]	ROM_ADDR_L	RW	flash-ROM address low byte	xxh

flash-ROM data register (ROM_DATA_HI, ROM_DATA_LO):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DATA_HH	RO	High byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_HL	RO	Low byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_LH	RO	High byte of flash-ROM data register low word (16 bits)	xxh
[7:0]	ROM_DATA_LL	RO	Low byte of flash-ROM data register low word (16 bits)	xxh

Buffer mode register for flash-ROM erase/program operation (ROM_BUF_MOD):

Bit	Name	Access	Description	Reset value
7	bROM_BUF_BYTE	RW	Buffer mode for flash-ROM erase/program operation: 0: Select the data block programming mode, and the data to be written is stored in xRAM pointed to by DPTR. During programming, CH545 automatically fetches data from xRAM in sequence and	x

			temporarily stores it in ROM_DAT_BUF and then writes into flash-ROM. It supports 1 to 64 bytes of data, and the actual length =MASK_ROM_ADR_END-ROM_ADDR_L[5:0]+1. 1: Select single-byte programming or 64-byte block erase mode. The data to be written is directly stored in ROM_DAT_BUF.	
6	Reserved	RW	Reserved	x
[5:0]	MASK_ROM_ADDR	RW	In flash-ROM data block programming mode, these bits are the lower 6 bits of the end address of the flash-ROM block programming operation (including such address). Reserved in flash-ROM single byte programming or 64-byte erase mode, and recommended to be 00h.	xxh

Data buffer register for flash-ROM erase/program operation (ROM_DAT_BUF):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DAT_BUF	RW	Data butter register for flash-ROM erase/program operation	xxh

flash-ROM control register (ROM_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

flash-ROM status register (ROM_STATUS):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	1
6	bROM_ADDR_OK	RO	flash-ROM operation address OK: 0: Invalid. 1: The address is valid	0
[5:2]	Reserved	RO	Reserved	0000b
1	bROM_CMD_ERR	RO	flash-ROM operation command error status bit: 0: The command is valid. 1: Unknown command, or overtime	0
0	Reserved	RO	Reserved	0

6.5 flash-ROM Operation Steps

1. Erase the flash-ROM, and change all data bits in the target block to 0:
   (1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
   (2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds to code or data).

(3). Set the address register (ROM_ADDR), to write a 16-bit target address, actually only the higher 10 bits are valid.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD) to 80h, to select 64-byte block erase mode.

(5). Optional, set the data buffer register for erase and write operation (ROM_DAT_BUF) to 00h.

(6). Set the operation control register (ROM_CTRL) to 0A6h, to execute block erase operation. The program is automatically suspended during operation.

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS) to check the status of the operation. If more than one block needs to be erased, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

2. Write to flash-ROM in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):

(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds to code or data).

(3). Set the address register (ROM_ADDR), to write a 16-bit target address.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD) to 80h, to select single byte programming mode.

(5). Set the data buffer register for erase/program operation (ROM_DAT_BUF) to the byte data to be written.

(6). Set the operation control register (ROM_CTRL) to 09Ah, to execute write operation. The program is automatically suspended during operation.

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS), to check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

3. Write to flash-ROM in block, change some data bits in several target bytes from 0 to 1 (the bit data cannot be changed from 1 to 0):

(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds to code or data).

(3). Set the address register (ROM_ADDR), to write a 16-bit start target address, such as 1357h.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD) to the lower 6 bits of the end target address (included), and such end address should be greater than or equal to the ROM_ADDR_L[5:0] start target address, to select the data block programming mode, for example, if the end address is 1364h, the ROM_BUF_MOD should be set to 24h (64h&3Fh), and the number of bytes of the data block =0Dh.

(5). In the xRAM, allocate a buffer area based on the alignment in 64 bytes, such as 0080h~00BFh, specify the offset address in such buffer area with the lower 6 bits of the start target address, to obtain the xRAM buffer start address of this data block programming operation, store the data block to be written from the xRAM buffer start address, and set the xRAM buffer start address into DPTR, e.g. DPTR=0080h+(57h&3Fh)=0097h, actually only the xRAM from 0097h to 00A4h addresses is used in this programming operation.

(6). Set the operation control register (ROM_CTRL) to 09Ah, to execute write operation. The program is automatically suspended during operation.

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS), to check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

4. Read flash-ROM:

Directly use MOVC command, or read the code/data of the target address through the pointer to the program address space.

5. Write to OTP data area in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):

(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bDATA_WE).

(3). Set the address register (ROM_ADDR), to write target address (20h~3Fh), actually only the higher 4 bits of the lower 6 bits are valid.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD) to 80h, to select single byte programming mode.

(5). Set the data buffer register for erase/program operation (ROM_DAT_BUF) to the byte data to be written.

(6). Set the operation control register (ROM_CTRL) to 099h, to execute write operation. The program is automatically suspended during operation;

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS), to check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

6. Read the ReadOnly information area or OTP data area in 4 bytes:

(1). Set the address register (ROM_ADDR), to write the target address based on the alignment in 4 bytes (00h~3Fh), actually only the lower 6 bits are valid.

(2). Set the operation control register (ROM_CTRL) to 08Dh, to execute read operation. The program is automatically suspended during operation.

(3). After the operation is completed, the program resumes running. In this case, you can inquire the

status register (ROM_STATUS), to check the status of the operation.

(4). Obtain 4-byte data from ROM_DATA_HI and ROM_DATA_LO in flash-ROM data register.

7. Notes: it is recommended that flash-ROM/EEPROM is erased/programmed only at the ambient temperature of -20°C ~ 85°C. If the erase/program operation is performed beyond the above temperature range, it is usually normal, but there may be the possibility of reducing data retention ability (TDR) and reducing the number of erase/program operations (NEPCE) or even affecting the accuracy of data.

6.6 On-board Program and ISP Download

When Code_Protect=0, the codes and data in CH543 flash-ROM can be read/written by an external programmer through the synchronous serial interface. When Code_Protect=1, the codes and data in the flash-ROM are protected and cannot be read out, but can be erased, and the code protection is removed when powered on again after erase operation.

When the CH543 is preset with BootLoader program, it supports various ISP download types, such as USB or UART to load the applications. But in the absence of a boot loader program, the boot loader program or application can only be written to CH543 by an external dedicated programmer. To support on-board program, 4 connection pins between the CH543 and the programmer should be reserved in the circuit. The 3 necessary connection pins are P1.4 (replaced with P3.6 and P3.7 when there is no P1.4), P1.6 and P1.7.

Table 6.6.1 Connection pins to the programmer

Pin	GPIO	Description
VDD	VDD12	It is required to control chip power in programming state.
SCS	P1.4	Chip Select input pin (necessary) in programming state. High level by default, active low.
SCK	P1.7	Clock input pin (necessary) in programming state
MISO	P1.6	Data output pin (necessary) in programming state

6.7 Unique ID

Each MCU has a unique ID when it is delivered from the factory, namely the chip identification number. This ID data and its checksum has 8 bytes in total, stored in the read-only information area at 10h offset address, please refer to the C Program Language routines for specific operations.

Table 6.7.1 Chip ID address table

Offset address	ID data description
10h,11h	ID first word data, correspond to the lowest byte and the second low byte of the ID number in order
12h,13h	ID secondary word data, correspond to the second high byte and high byte of the ID number in order
14h,15h	ID last word data, correspond to the second highest byte and the highest byte of the 48-bit ID number in order
16h,17h	16-bit cumulative sum of ID first word, secondary word, last word data, used for ID check

The ID number can be used with the download tools to encrypt the target program. For the general applications, only the first 32 bits of the ID number are used.

7. Power Management, Sleep and Reset

7.1 External Power Input

The CH543 has a built-in 12V to 3.3V low dropout voltage regulator (LDO), and the generated 3.3V power supply is used for USB and I/O supply. LDO can also generate 4.7V power, but the USB communication is not supported, others are the same as 3.3V. The P3.5 pin select VDD12 as I/O supply, ans supports high-voltage input/output. Other I/O pins use VDD as I/O supply. CH543 supports external 5V, 9V or 3.3V, or even 12V, 2.8V power input. Refer to the following table for the two supply voltage input modes.

External supply voltage	Voltage on VDD12: Support up to 12.6V external voltage	Voltage on VDD: Support up to 5.5V I/O voltage (Note: VDD is shorted to VDD12 during sleep)
Rated 3.3V, 2.8V~5.5V supported	Input external power supply to voltage regulator. It is recommended to be connected with a decoupling capacitor (not less than 0.1uF) to ground. It is recommended to connect 1uF or more decoupling capacitor to ground.	VDD12 input shorted as I/O and USB power. Must be connected with a decoupling capacitor (not less than 0.1uF) to ground. It is recommended to connect a 1uF decoupling capacitor to ground.
Rated 5V, 4V~6V supported	Input external high voltage to voltage regulator. Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.	Internal LDO output, and I/O and USB power input. Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.
5V, 9V, 12V, 4V to 12.6V supported	The input external high voltage to the voltage regulator must be connected to a decoupling capacitor of not less than 10uF to the ground	The internal LDO output and I/O and USB power input must be connected to a decoupling capacitor of not less than 1uF to the ground

After power on reset or system reset, CH543 is in running state by default. On the premise that the performance meets the requirements, the power consumption can be reduced during operation by appropriately reducing the system clock frequency. When CH543 does not need to run at all, PD in PCON can be set to sleep. In Sleep mode, external wakeup can be implemented via USB, USB PD, UART0, I2C, SPI0 and part of GPIOs.

7.2 Power Supply and Sleep Control Register

Table 7.2.1 Power supply and sleep control registers

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
POWER_CFG	BAh	Power management configuration register	0xh
WAKE_CTRL	A9h	Wakeup control register	00h
PCON	87h	Power control register	10h

Watchdog count register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Current count of watchdog. It overflows when the count is full from 0FFh to 00h, and the bWDOG_IF_TO interrupt flag is automatically set to 1 during overflow.	00h

Power management configuration register (POWER_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	MASK_SLP_MODE	RW	Sleep power down mode selection, enabled by setting the PD bit: 00: Select shutdown / deep-sleep mode. All power OFF. It can save more power but wake up the slowlest. 01: Select sleep mode. flash-ROM and clock OFF. It can save power, but wake up slowly. 10: Select halt mode. Only clock OFF. It can wake up quickly. 11: Select idle mode. Clock does not stop. It can wake up immediately.	00b
5	bLDO_3V3_SEL	RW	Select the output voltage on VDD from the internal voltage regulator: 0: 3.3V selected. 1: 4.7V selected.	0
4	bLDO_3V3_OFF	RW	LDO OFF control (auto OFF during sleep): 0: 3.3V generated by VDD12 supply for I/O, USB and other modules. 1: LDO disabled. VDD internally shorted to VDD12.	0
3	bLDO_CORE_VOL	RW	Cor voltage mode: 0: Normal voltage. 1: Boost voltage mode. Performance is better and a higher clock frequency is supported.	0
[2:0]	MASK_ULLDO_VOL	RW	Data retention supply voltage selection in shutdown /deep-sleep mode: 000: 1.5V selected. 001: 1.57V selected. 010: 1.64V selected. 011: 1.71V selected. 100: 1.78V selected. 101: 1.85V selected. 110: 1.92V selected. 111: 1.99V selected.. The above values are for reference only and not recommended to modify.	xxxb

Wakeup control register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bWAK_BY_USB	RW	USB event wakeup enable 0: USB event wakeup disabled.	0

6	bWAK_P1_7_LO	RW	P1.7 low level wakeup enable 0: P1.7 low level wakeup disabled.	0
5	bWAK_P1_5_LO	RW	P1.5 low level wakeup enable 0: P1.5 low level wakeup disabled.	0
4	bWAK_P1_4_LO	RW	P1.4 low level wakeup enable 0: P1.4 low level wakeup disabled.	0
3	bWAK_P1_3_LO	RW	P1.3 low level wakeup enable 0: P1.3 low level wakeup disabled.	0
2	bWAK_P3_3_LO	RW	P3.3 low level wakeup enable 0: P3.3 low level wakeup disabled.	0
1	bWAK_INT0_EDGE	RW	INT0 edge change wakeup enable 0: INT0 edge change wakeup disabled. Select either INT0 or INT0_ pin based on bINT0_PIN_X=0/1	0
0	bWAK_RXD0_LO	RW	UART0 receive input low level wakeup enable 0: UART0 receive input low level wakeup disabled. Select RXD or RXD_ or RXD10_ or RXD11_ based on MASK_UART_I2C=00/01/10/11.	0

Other signal sources that can wake up the chip include:

When bWAK_BY_USBPD=1, either USB PD or USB type C event can wake up the chip.

When En_RST_RESET=1, high level on the RST pin can wakeup and reset the chip.

When En_RST_RESET=0, bRST_ANA=0, bRST_VOL_SEL=1, bRST_PD1=1 and bRST_PD0=1, high level on the RST pin can wake up the chip.

Power control register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	When the UART0 baud rate is generated by timer 1, select the communication baud rate of UART0 mode 1, 2 and 3: 0: Slow mode. 1: Fast mode	0
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	RO	Last reset flag high bit	0
4	bRST_FLAG0	RO	Last reset flag low bit	1
3	GF1	RW	General flag bit 1 User-defined. Reset and set by software.	0
2	GF0	RW	General flag bit 0 User-defined. Reset and set by software.	0
1	PD	RW	Sleep mode enable Sleep after set to 1. Automatically reset by hardware after wakeup. It is strongly recommended to disable the global interrupt before sleep (EA=0).	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Last reset flag description

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset Source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1). Or USB PD reset signal when bPD_RST_EN=1.
0	1	Power on reset or low voltage reset or over-voltage reset Source: VDD12 voltage detection.
1	0	Watchdog reset Source: bWDOG_EN=1 and watchdog timeout overflows.
1	1	External pin manual reset Source: En_RST_RESET=1 and RST input high level.

7.3 Reset Control

CH543 supports 7 reset sources: power on reset, power supply low voltage reset, power supply over-voltage reset, external reset, software reset, USB PD reset signal and watchdog reset. The last 4 are thermal resets.

7.3.1 Power on Reset, Low Voltage Reset and Over-voltage Reset

The power on reset (POR) is generated by the on-chip power-on detection circuit. Automatically delay Tpor through hardware to keep reset. After the delay, the CH543 runs.

Low voltage reset (LVR) is generated by the on-chip voltage detection circuit. The LVR circuit continuously monitors the supply voltage on the VDD12 pin. When it is lower than the detection voltage (Vpot), the low voltage reset occurs and it automatically delays Tpor through hardware to keep reset. After the delay, the CH543 runs.

Over-voltage reset (OVR) is generated by the on-chip high voltage detection circuit. The OVR circuit continuously monitors the supply voltage on the VDD12 pin. When it is higher than the detection voltage (Vovr), the over-voltage reset occurs and it automatically delays Tpor through hardware to keep reset. After the delay, the CH543 runs.

Only power on reset, low voltage reset and over-voltage reset can enable CH543 to reload the configuration information. Other thermal resets do not affect it.

7.3.2 External Reset

The external reset is generated by the low level applied to the RST# pin externally. The reset is triggered when En_P71_RESET is 1 and the low level duration on the RST# pin is greater than Trst. When the external low level signal is canceled, automatically delay Trdl by hardware to keep reset. After the delay, CH543 executes from address 0.

7.3.3 Software Reset

CH543 supports internal software reset, so that the CPU can be actively reset and re-run without external intervention. Set bSW_RESET in global configuration register (GLOBAL_CFG) to 1 to generate software reset, and automatically delay Trdl to keep reset. After the delay, CH543 executes from address 0, and the bSW_RESET bit is cleared automatically by hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, bRST_FLAG1/0 indicates a software reset after reset. When bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, bRST_FLAG1/0 remains the previous reset flag rather than generate a new one.

For a chip with ISP boot loader, the boot loader firstly runs after power on reset, and the program reset the chip as needed to switch to the application state. In this case, software reset only causes that bBOOT_LOAD is cleared, and it does not affect bRST_FLAG1/0 (as bBOOT_LOAD=1 before reset) , so when switching to the application state, bRST_FLAG1/0 still indicates the power on reset state.

7.3.4 USB PD Reset Signal

When bPD_RST_EN=1, CH543 supports reset which is generated by the USB PD Hard Reset signal frame. If bPIE_RX_RST is also 1, CH543 also supports reset which is generated by the Cable Reset signal frame. Reset flag generated by USB PD is the same as software reset.

7.3.5 Watchdog Reset

Watchdog reset is generated when the watchdog timer overflows. The watchdog timer is an 8-bit counter, whose count clock frequency is Fsys/131072, and the overflow signal is generated when the count reaches 0FFh and turns to 00h.

The watchdog timer overflow signal triggers the interrupt flag (bWDOG_IF_TO) to 1, which is automatically cleared when WDOG_COUNT is reloaded or when it enters the corresponding interrupt service program.

Different timing cycles (Twdc) are achieved by writing different count initial values to WDOG_COUNT. When the system clock frequency is 12MHz, the watchdog timing cycle (Twdc) is about 2.8 s when 00h is written, and about 1.4 s when 80h is written.

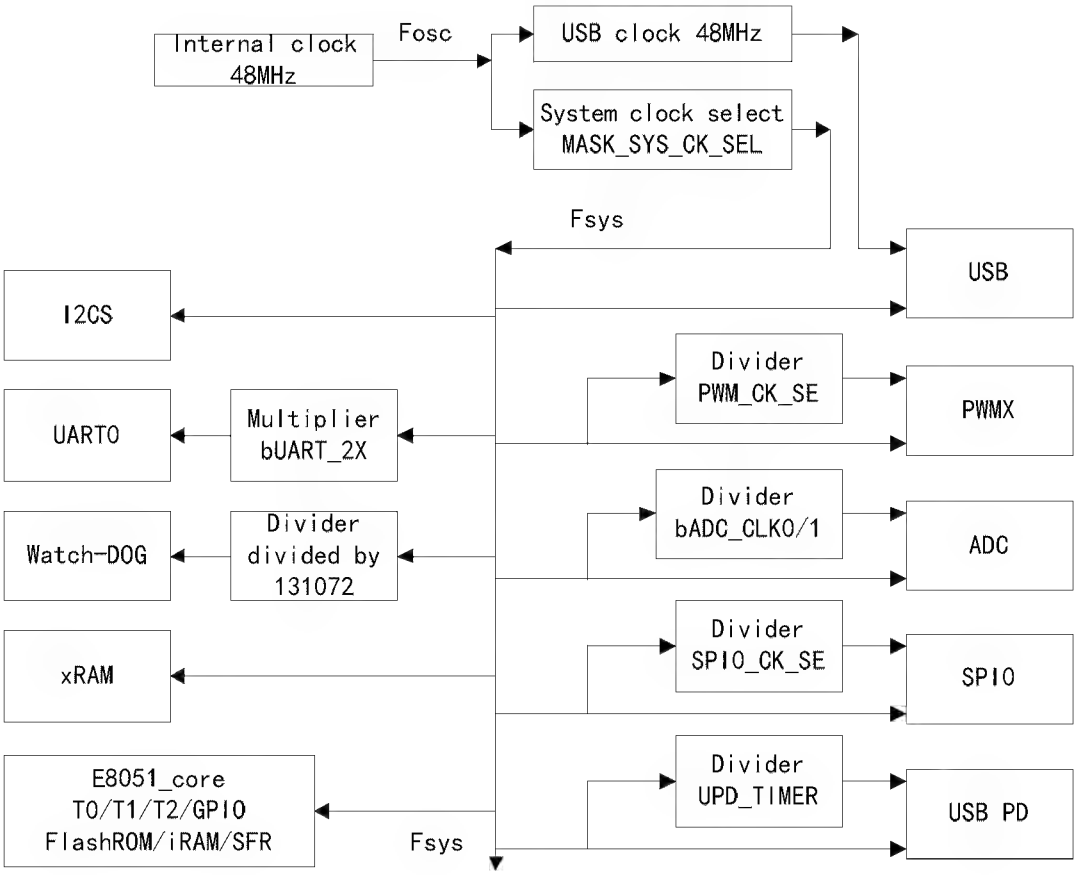
If bWDOG_EN=1 when watchdog timer overflows, watchdog reset occurs, and automatically delay Trdl to keep reset. After the delay, CH543 executes from address 0.

When bWDOG_EN=1, to avoid watchdog reset, WDOG_COUNT must be reset timely to avoid its overflow.

8. System Clock

8.1 Clock Block Diagram

Figure 8.1.1 Clock system and structure diagram



The internal clock is the original clock (Fosc), also is the clock of USB module (Fusb4x). The system clock frequency (Fsys) is obtained through divider. Fsys is directly provided for each module of CH543.

8.2 Register Description

Table 8.2.1 Clock control register

Name	Address	Description	Reset value
CLOCK_CFG	B9h	System clock configuration register	03h

System clock configuration register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUSB_CLK_EN	RW	USB clock enable: 0: USB clock disabled to reduce power consumption. 1: USB clock enabled. USB clock is automatically enabled after it accesses	0

			USB register twice.	
5	bWDOG_IF_TO	RO	Watchdog timer interrupt flag bit 1: Interrupt triggered by the timer overflow signal. 0: No interrupt. This bit is automatically cleared when the watchdog count register (WDOG_COUNT) is reloaded or after it enters the corresponding interrupt service program.	0
4	bUART_2X	RW	UART0 multiplier mode: 0: Fsys used as the reference clock. A normal baud rate is generated. 1: Fsys x 2 used. A double baud rate is generated.	0
3	Reserved	RO	Reserved	0
[2:0]	MASK_SYS_CK_SEL	RW	System clock selection. Refer to Table 8.2.2.	011b

Table 8.2.2 System clock selection table

MASK_SYS_CK_SEL	System clock frequency (Fsys)	Fsys frequency	Description
000b	Fosc / 128	~5KHz	Low frequency. The error is larger but it can save power.
001b	Fosc / 128	375KHz	
010b	Fosc / 16	3MHz	
011b	Fosc / 4	12MHz	
100b	Fosc / 3	16MHz	
101b	Fosc / 2	24MHz	Reduce wakeup delay. Wake up quickly.
110b	Fosc / 2	24MHz	Wake up normally.
111b	Fosc / 1	48MHz	For CH541 chips, use is prohibited. For custom CH543 chips, 48MHz, with bLDO_CORE_VOL set to 1. 48MHz has a narrow temperature range and is only available for special use with CH543 custom chips.

8.3 Clock Configuration

CH543 defaults to use the internal clock after power on. The internal clock frequency is 48MHz.

Original clock frequency: Fosc = MASK_SYS_CK_SEL != 000 ? 48MHz : ~400KHz.

USB clock frequency: Fusb4x = Fosc.

For Fsys, please refer to Table 8.2.2, and it is obtained based on divided Fosc.

After reset, Fosc=48MHz, Fusb4x=48MHz, Fsys=12MHz by default.

Steps for modifying the system clock frequency:

(1). Enter the safe mode: SAFE_MOD = 55h firstly; then SAFE_MOD = AAh.

(2). Write a new value to CLOCK_CFG.

(3). Terminate the safe mode: write any value into SAFE_MOD to prematurely terminate the safe mode.

Notes:

(1). When the full-speed USB is used, Fsys is not less than 6MHz. When the low-speed USB is used, Fsys is not less than 3MHz.

(2). The accuracy of the internal clock is not high, and it may not be suitable for USB host applications or high-requirement USB device applications.

(3). A lower system clock frequency (Fsys) is preferred to reduce the system dynamic power consumption and widen the operating temperature range.

9. Interrupt

CH543 supports 16 interrupt signal souces which consist of 6 interrupts ((INT0, T0, INT1, T1, UART0 and T2) compatible with standard MCS51, and 9 extended interrupts (SPI0, I2C, USB, ADC, USB PD, PWMX/CMP, GPIO and WDOG). The GPIO interrupt can be selected from several I/O pins. The USB interrupr is P3.6/P3.7 level change interrupt when USB is disabled and GPIO is enabled. The USB PD interrupt is P1.0/P1.1 level change interrupt when USB PD is disabled and GPIO is enabled.
Interrupt service programs should be as compact as possible. If possible, avoid calling functions and subroutines as well as reading/writing xdata variables and code constants.

9.1 Register Description

Table 9.1.1 Interrupt vector table

Interrupt source	Entry address	Interrupt No.	Description	Default priority sequence
INT_NO_INT0	0x0003	0	External interrupt 0	High priority ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ Low priority
INT_NO_TMR0	0x000B	1	Timer 0 interrupt	
INT_NO_INT1	0x0013	2	External interrupt 1	
INT_NO_TMR1	0x001B	3	Timer 1 interrupt	
INT_NO_UART0	0x0023	4	UART0 interrupt	
INT_NO_TMR2	0x002B	5	Timer 2 interrupt	
INT_NO_SPI0	0x0033	6	SPI0 interrupt	
INT_NO_I2C	0x003B	7	I2C interrupt	
INT_NO_USB	0x0043	8	USB interrupt, P3.6/P3.7 level change interrupt	
INT_NO_ADC	0x004B	9	ADC/TKEY interrupt	
INT_NO_USBPD	0x0053	10	USBPD interrupt, P1.0/P1.1 level change interrupt	
INT_NO_PWMX INT_NO_CMP	0x005B	11	PWMX/CMP interrupt Analyze based on bPWM_IE_END and bCMP_IE	
INT_NO_GPIO	0x0063	12	GPIO interrupt	
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 Interrupt registers

Name	Address	Description	Reset value
IP_EX	E9h	Extend interrupt priority control register	00h
IE_EX	E8h	Extend interrupt enable register	00h
GPIO_IE	B2h	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
IE	A8h	Interrupt enable register	00h

Interrupt enable register (IE):

Bit	Name	Access	Description	Reset

				value
7	EA	RW	Global interrupt enable bit 1: Interrupt enabled when E_DIS is 0. 0: All interrupts requests are masked.	0
6	E_DIS	RW	Global interrupt disable bit 1: All interrupts requests are masked. 0: Interrupt enabled when EA is 1. This bit is usually used to temporarily disable the interrupt during flash-ROM operation.	0
5	ET2	RW	Timer 2 interrupt enable bit 1: T2 interrupt enabled. 0: Interrupt request is masked.	0
4	ES	RW	UART0 interrupt enable bit 1: UART0 interrupt enabled. 0: Interrupt request is masked.	0
3	ET1	RW	Timer 1 interrupt enable bit 1: T1 interrupt enabled. 0: Interrupt request is masked.	0
2	EX1	RW	External interrupt 1 enable bit 1: INT1 interrupt enabled. 0: Interrupt request is masked.	0
1	ET0	RW	Timer 0 interrupt enable bit 1: T0 interrupt enabled. 0: Interrupt request is masked.	0
0	EX0	RW	External interrupt 0 enable bit 1: INT0 interrupt enabled. 0: Interrupt request is masked.	0

Extend interrupt enable register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable bit 1: WDOG interrupt enabled. 0: Interrupt request is masked.	0
6	IE_GPIO	RW	GPIO interrupt enable bit 1: Interrupt in GPIO_IE enabled. 0: All interrupts in GPIO_IE are masked.	0
5	IE_PWMX IE_CMP	RW	PWMX, CMP interrupt enable bit 1: PWMX, CMP interrupt enabled. 0: Interrupt request is masked.	0
4	IE_USBPD	RW	USB PD interrupt enable bit 1: USB PD interrupt enabled. 0: Interrupt request is masked.	0
3	IE_ADC	RW	ADC interrupt enable bit	0

			1: ADC interrupt enabled. 0: Interrupt request is masked.	
2	IE_USB	RW	USB interrupt enable bit 1: USB interrupt enabled. 0: Interrupt request is masked.	0
1	IE_I2C	RW	I2C Slave interrupt enable bit 1: I2C Slave interrupt enabled. 0: Interrupt request is masked.	0
0	IE_SPI0	RW	SPI0 interrupt enable bit 1: SPI0 interrupt enabled. 0: Interrupt request is masked.	0

GPIO interrupt enable register (GPIO_IE), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: 0: Level interrupt mode selected. If the GPIO pin inputs a valid level, bIO_INT_ACT is 1 and always requests interrupt. If GPIO inputs an invalid level, bIO_INT_ACT is 0 and the interrupt request is canceled. 1: Edge interrupt mode selected. When GPIO pin inputs a valid edge, the bIO_INT_ACT interrupt flag is generated and an interrupt is requested. The interrupt flag cannot be cleared by software and can only be cleared automatically when reset or in level interrupt mode or when it enters the corresponding interrupt service program.	0
6	bIE_P1_7_LO	RW	1: P1.7 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.7 interrupt disabled.	0
5	bIE_P1_5_LO	RW	1: P1.5 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.5 interrupt disabled.	0
4	bIE_P1_4_LO	RW	1: P1.4 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.4 interrupt disabled.	0
3	bIE_P1_3_LO	RW	1: P1.3 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.3 interrupt disabled.	0
2	bIE_RST_HI	RW	1: RST interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: RST interrupt disabled.	0
1	bIE_P3_1_LO	RW	1: P3.1 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: : P3.1 interrupt disabled.	0
0	bIE_RXD0_LO	RW	1: UART0 receive pin interrupt enabled(active at low level in	0

			level mode, while active at falling edge in edge mode). 0: UART0 receive pin interrupt disabled. Select RXD or RXD_ or RXD10_ or RXD11_ based on MASK_UART_I2C=00/01/10/11.	

Interrupt priority control register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	Flag bit for high-priority interrupt in progress	0
6	PL_FLAG	RO	Flag bit for low-priority interrupt in progress	0
5	PT2	RW	Timer 2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer 1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 interrupt priority control bit	0
1	PT0	RW	Timer 0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 interrupt priority control bit	0

Extend interrupt priority control register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nested level flag bit 0: No interrupt, or 2-level nested interrupt. 1: Current 1-level nested interrupt	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX bIP_CMP	RW	PWMX, CMP interrupt priority control bit	0
4	bIP_USBPD	RW	USB PD interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_I2C	RW	I2C interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

IP and IP_EX are used to set the interrupt priority. If a bit is set to 1, then the corresponding interrupt source is set to high-priority. If a bit is cleared, then the corresponding interrupt source is set to low-priority. For the interrupt sources at the same level, the system has a priority sequence by default, as shown in Table 9.1.1. The combination of PH_FLAG and PL_FLAG represents the priority of interrupts.

Table 9.1.3 Current interrupt priority state indication

PH_FLAG	PL_FLAG	Current interrupt priority state
0	0	No interrupt at present
0	1	Low-priority interrupt is executed at present
1	0	High-priority interrupt is executedg at present
1	1	Unexpected state, unknown error

10. I/O Ports

10.1 GPIO Introduction

CH543 provides up to 17 I/O pins. Some pins have alternate functions. The inputs and outputs except for RST can be accessed by bits.

If a pin is not configured with alternate functions, it is a general purpose I/O pin by default. When used as general purpose digital I/O ports, all of them have a real "read-modify-write" function that allows SETB, CLR and other bit operation commands to independ ently change the direction and port level of a pin.

Note: P1.0 and P1.1 both have a current anti-backflow circuit, and they do not support VDD full-width voltage output.

10.2 GPIO Register

All registers and bits in this section are represented in a generic format: a lowercase "n" represents the serial number of ports (n=1, 3) , and a lowercase "x" represents the serial number of bits (x=0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 GPIO registers

Name	Address	Description	Reset value
PIN_MISC	91h	CH543: Miscellaneous I/O control register	80h
		CH541: Miscellaneous I/O control register	00h
P1	90h	P1 port input/output register	FFh
P1_DIR_PU	93h	CH543: P1 port direction control and pull-up enable register	70h
		CH541: P1 port direction control and pull-up enable register	F0h
P1_MOD_OC	92h	P1 port output mode register	FFh
P1_ANA_PIN	94h	P1 port analog mode control register	00h
P3	B0h	P3 port input/output register	FFh
P3_DIR_PU	97h	P3 port direction control and pull-up enable register	FFh
P3_MOD_OC	96h	P3 port output mode register	FFh
P3_ANA_PIN	95h	P3 port analog mode control register	00h
XBUS_AUX	A2h	External bus auxiliary setting register	00h
PIN_FUNC	AAh	Pin function selection register	00h
PIN_RST	B3h	RST pin configuration register	07h

Pn port input/output register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0～Pn.7	RW	Pn.x pin state input and data output bits. Can be accessed by bits	FFh

Pn port output mode register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0: Push-pull output. 1: Open-drain output.	FFh

Pn port direction control and pull-up enable register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR_PU	RW	Pn.x pin direction control in push-pull output mode: 0: Input. 1: Output. Pn.x pin pull-up resistor enable control in open-drain output mode: 0: Pull-up resistor disabled. 1: Pull-up resistor enabled. Exception: PD output, USB output and SPI slave output (MISO) are driven by the controller to output. So they are not required to be set to output here. P1.0, P1.1, P3.6 and P3.7 pull-up resistors are not controlled here. Refer to CC1_CTRL, CC2_CTRL and USB_PULL.	CH543 P1:70h CH541 P1: F0h For P3: FFh

P1 port analog mode control register (P1_ANA_PIN):

Bit	Name	Access	Description	Reset value
[7:0]	bP1_x_ANA	RW	P1.x pin analog mode setting: 0: Analog bidirectional / digital input and output enabled. 1: Analog bidirectional / digital output enabled, digital input disabled to save power consumption.	00h

P3 port analog mode control register (P3_ANA_PIN):

Bit	Name	Access	Description	Reset value
7	bP3_7_ANA	RW	P3.7 pin analog mode setting: 0: Analog bidirectional / digital input and output enabled. 1: Analog bidirectional / digital output enabled, digital input disabled to save power consumption.	0
6	bP3_6_ANA	RW	P3.6 pin analog mode setting: 0: Analog bidirectional / digital input and output enabled. 1: Analog bidirectional / digital output enabled, digital input disabled to save power consumption.	0
[5:3]	Reserved	RO	Reserved	000b
2	bP3_2_ANA	RW	P3.2 pin analog mode setting: 0: Analog bidirectional / digital input and output enabled. 1: Analog bidirectional / digital output enabled, digital	0

			input disabled to save power consumption.	
1	bUSB_OUT_VOL1	RW	MASK_USB_OUT_VOL select to output static voltage on DP/DM to support BC and other charging protocols: 00: Output voltage disabled. 01: Output around 0.6V on DM when bUDP_PDE=1. Output around 0.6V on DP when bUDM_PDE=1. DP is internally shorted to DM when bUDP_PDE=0 and bUDM_PDE=0. Support CDP and DCP. 10: Output around 1.2V on DP and DM simultaneously. 11: Output around 2.7V on DP and DM simultaneously.	0
0	bUSB_OUT_VOL0	RW		0

Relevant configuration of Pn port is implemented by the combination of Pn_MOD_OC[x] and Pn_DIR_PU[x].

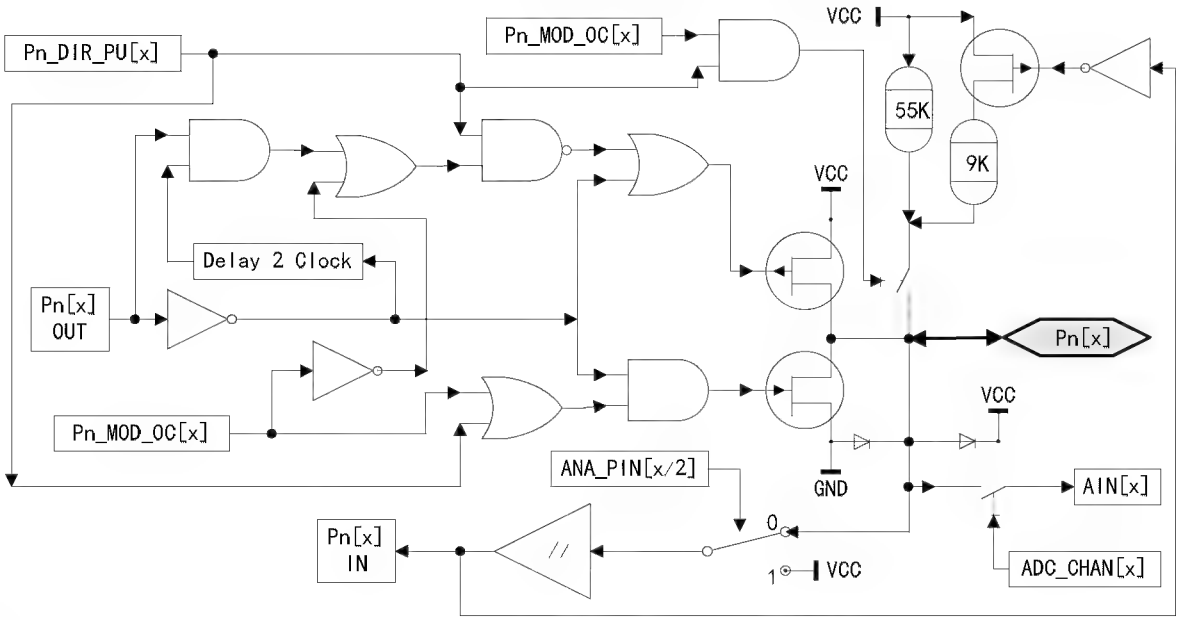
Table 10.2.2 Port configuration register combination

Pn_MOD_OC	Pn_DIR_PU	Operating mode description (P1.0/P1.1/P3.6/P3.7 pull-up resistors are controlled in other ways)
0	0	High impedance input mode, the pin has no pull-up or pull-down resistor.
0	1	Push-pull output mode, the pin has symmetrical drive capability, and can output or sink large current.
1	0	Open-drain output. High impedance input is supported, the pin has no pull-up resistor.
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, supports input, the pin has pull-up resistor. When the output is changed from low level to high level, it automatically drives the high level for 2 clock cycles to accelerate the conversion

P1 and P3 ports support pure input, push-pull output and quasi-bidirectional mode. Each pin has an internal pull-up resistor which can be controlled freely (Exception: The values of P1.0, P1.1, P3.6 and P3.7 pull-up resistors are different, and these resistors need to be controlled in other ways). Each pin has a protection diode connected to VDD and GND (Exception: P1.0, P1.1 and RST are not connected with diodes to VDD. The external voltage which is higher than VDD will not cause sink current to VDD). The output PMOS and the diode of P3.5 are not connected to VDD, but connected to VDD12.

Figure 10.2.1 shows the schematic diagram of P1.x pins of P1 port and P3.x pins of P3 port. Some pins do not support analog input, without AIN, ADC_PIN or ADC_CHAN.

Figure 10.2.1 I/O pin schematic diagram



RST pin configuration register (PIN_RST):

Bit	Name	Access	Description	Reset value
7	bIO_INT_ACT	RO	GPIO interrupt request activate state: When bIE_IO_EDGE=0, 1: GPIO input active level. Interrupt to be requested. 0: GPIO input inactive level. When bIE_IO_EDGE=1, this bit acts as edge interrupt flag. If this bit is 1, an active edge is detected. This bit cannot be cleared by software, but can be automatically cleared when reset or in level interrupt mode or when it enters the corresponding interrupt service program.	0
6	bRST	RO	RST pin status input bit	0
[5:4]	Reserved	RO	Reserved	00b
3	bRST_ANA	RW	RST pin analog mode setting: 0: Analog bidirectional and digital input enabled. 1: Analog bidirectional enabled, digital input disabled to save power consumption.	0
2	bRST_VOL_SEL	RW	RST pin analog voltage ratio and pull-down resistor setting: 0: No pull-down resistor. Pin voltage is directly used for analog. 1: 40KΩ pull-down resistor enabled. Pin voltage dropped to 25% and then used for analog.	1
[1:0]	MASK_RST_PD	RW	RST pin pull-down current selection: 00: Pull-down / sink current disabled.	11b

			01: Pulled down about 8mA (14mA@VDD=4V7). It is not recommended to discharge continuously. 10: Pulled down about 1.4mA (2.3mA@VDD=4V7). 11: Pulled down about 5uA when bRST_VOL_SEL=0. Otherwise combines.	

Miscellaneous I/O control register (PIN_MISC):

Bit	Name	Access	Description	Reset value
7	bP1_7_WPU	RW	P1.7 weak pull-up current enable (Only for CH543. Always 0 for CH541): 0: P1.7 weak pull-up current disabled 1: P1.7 weak pull-up current enabled, about 5uA.	1
6	bVHV_SINK	RW	VDD12 discharge current (current consumed) enable (Only for CH543): 0: VDD12 discharge current disabled. 1: VDD12 discharge current enabled, about 6.6mA (9mA@VDD=4V7).	0
5	bP3_5_PDE	RW	P3.5 pull-down resistor / current enable: 0: P3.5 pull-down disabled. 1: P3.5 pull-down resistor / current enabled (40~300uA)	0
4	bINT0_POLAR	RW	INT0 or INT0_ signal polarity selection: 0: Active low (falling edge). 1: Active high (rising edge).	0
3	bWAK_BY_USBPD	RW	USB PD or type C event wakeup enable 0: USB PD or type C event wakeup disabled.	0
[2:0]	Reserved	RO	Reserved	000b

10.3 GPIO Alternate Functions and Map

Some I/O pins of CH543 have alternate functions. After power on, they act as all general-purpose I/O pins by default. After different functional modules are enabled, the corresponding pins are configured as corresponding functional pins of each functional module.

Pin function selection register (PIN_FUNC):

Bit	Name	Access	Description	Reset value
7	bPWM1_PIN_X	RW	PWM1 pin mapping enable bit 0: P3.4. 1: P3.1.	0
6	bPWM0_PIN_X	RW	PWM0 pin mapping enable bit 0: P1.5. 1: P3.0.	0
5	bPWM2_PIN_X	RW	PWM2 pin mapping enable bit 0: P1.6. 1: P3.3.	0

4	bUART0_PIN_X	RW	MASK_UART_I2C select mapping mode of UART0 pins and I2C pins: 00: RXD/TXD uses P3.0/P3.1. SCL/SDA uses P1.6/P1.7. 01: RXD/TXD uses P1.6/P1.7. SCL/SDA uses P3.0/P3.1. 10: RXD/TXD uses P3.6/P3.7. SCL/SDA uses P1.6/P1.7. 11: RXD/TXD uses P3.7/P3.6. SCL/SDA uses P1.6/P1.7.	00b
3	bI2C_PIN_X	RW		
2	bINT0_PIN_X	RW	INT0 pin mapping enable bit 0: P3.2. 1: P1.2.	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable bit 0: P1.1. 1: RST.	0
0	bT2_PIN_X	RW	T2/CAP1 pin mapping enable bit 0: P1.0. 1: P1.4.	0

Table 10.3.1 Alternate functions of GPIO pins

GPIO	Other functions: priority sequence from left to right
P1[0]	CC1/bCC1, T2/bT2, CAP1/bCAP1, AIN0, P1.0
P1[1]	CC2/bCC2, T2EX/bT2EX, CAP2/bCAP2, AIN1, P1.1
P1[2]	INT0_/bINT0, AIN10, CO/bCO, P1.2
P1[3]	AIN11, CM/bCM, P1.3
P1[4]	T2_/bT2_, CAP1_/bCAP1_, SCS/bSCS, PWM3/bPWM3, AIN4, P1.4
P1[5]	MOSI/bMOSI, PWM0/bPWM0, AIN5, P1.5
P1[6]	MISO/bMISO, SCL/bSCL, RXD_/bRXD_, PWM2/bPWM2, AIN6, P1.6
P1[7]	SCK/bSCK, SDA/bSDA, TXD_/bTXD_, AIN7, P1.7
P3[0]	RXD/bRXD, PWM0_/bPWM0_, SCL_/bSCL_, P3.0
P3[1]	TXD/bTXD, PWM1_/bPWM1_, SDA_/bSDA_, P3.1
P3[2]	INT0/bINT0, AIN2, P3.2
P3[3]	INT1/bINT1, PWM2_/bPWM2_, P3.3
P3[4]	T0/bT0, PWM1/bPWM1, P3.4
P3[5]	T1/bT1, HVIO/bHVIO, P3.5
P3[6]	bDP/bDP, TXD11, RXD10, AIN8, P3.6
P3[7]	bDM/bDM, TXD10, RXD11, AIN9, P3.7
RST	bT2EX_, bCAP2_, bAIN3, bCP, bRST

The priority sequence from left to right mentioned in the above table refers to the priority when several functional modules compete to use a GPIO.

11. External Bus (xBUS)

CH543 does not provide bus signals for the outside, and the external bus is not supported, but the on-chip xRAM can be accessed normally.

External bus auxiliary setting register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	RO	UART0 transmit status If this bit is 1, the transmission is in progress.	0
6	bUART0_RX	RO	UART0 receive status If this bit is 1, the reception is in progress.	0
5	bSAFE_MOD_ACT	RO	Safe mode activate status If this bit is 1, it is in safe mode currently.	0
4	Reserved	RO	Reserved	0
3	GF2	RW	General flag bit 2 User-defined. Cleared and set by software.	0
2	bDPTR_AUTO_INC	RW	Enable the DPTR to add 1 automatically at the end of MOVX_@DPTR command	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Dual DPTR data pointer selection bit: 0: DPTR0 selected. 1: DPTR1 selected.	0

12. Timer

12.1 Timer0/1

Timer0 and Timer1 are 2 16-bit timers/counters which are configured by TCON and TMOD. TCON is used for timer/counter T0 and T1 startup control and overflow interrupt as well as external interrupt control. Each timer is a 16-bit timing unit composed of 2 8-bit registers. The high byte counter of Timer 0 is TH0 and the low byte counter of Timer 0 is TL0. The high byte counter of Timer 1 is TH1 and the low byte counter of Timer 1 is TL1. Timer 1 can also be used as the baud rate generator of UART0.

Table 12.1.1 Timer0/1 registers

Name	Address	Description	Reset value
TH1	8Dh	Timer 1 count high byte	00h
TH0	8Ch	Timer 0 count high byte	00h
TL1	8Bh	Timer 1 count low byte	00h
TL0	8Ah	Timer 0 count low byte	00h
TMOD	89h	Timer0/1 mode register	00h
TCON	88h	Timer0/1 control register	00h

Timer/counter 0/1 control register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag bit Automatically cleared after it enters Timer1 interrupt.	0
6	TR1	RW	Timer1 startup/stop bit Set to 1 to startup. Set and cleared by software.	0
5	TF0	RW	Timer0 overflow interrupt flag bit Automatically cleared after it enters Timer0 interrupt.	0
4	TR0	RW	Timer0 startup/stop bit Set to 1 to startup. Set and cleared by software.	0
3	IE1	RW	INT1 interrupt request flag bit Automatically cleared after it enters INT1 interrupt.	0
2	IT1	RW	INT1 trigger mode control bit 0: INT1 triggered by low level. 1: INT1 triggered by falling edge.	0
1	IE0	RW	INT0 interrupt request flag bit Automatically cleared after it enters INT0 interrupt.	0
0	IT0	RW	INT0 trigger mode control bit 0: INT0 triggered by low level. 1: INT0 triggered by falling edge.	0

Timer/counter 0/1 mode register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Gate control enable bit. This bit controls whether the Timer1 startup is affected by INT1. 0: Whether the timer/counter 1 is started is independent of INT1. 1: It is started only when the INT1 pin is at high level and TR1 is 1.	0
6	bT1_CT	RW	Timing/counting mode selection bit 0: It works in timing mode. 1: It works in counting mode. Falling edge on T1 pin selected as the clock.	0
5	bT1_M1	RW	Timer/counter 1 mode selection high bit	0
4	bT1_M0	RW	Timer/counter 1 mode selection low bit	0
3	bT0_GATE	RW	Gate control enable bit. This bit controls whether the Timer0 startup is affected by INT0. 0: Whether the timer/counter 0 is started is independent of INT0. 1: It is started only when the INT0 pin is at high level and TR0 is 1	0
2	bT0_CT	RW	Timing/counting mode selection bit 0: It works in timing mode. 1: It works in counting mode. Falling edge on T0 pin selectd as the clock	0
1	bT0_M1	RW	Timer/counter 0 mode selection high bit	0
0	bT0_M0	RW	Timer/counter 0 mode selection low bit	0

Table 12.1.2 Timern working mode selected by bTn_M1 and bTn_M0 (n=0, 1)

bTn_M1	bTn_M0	Timern working mode (n=0, 1)
0	0	Mode 0: 13-bit timer/counter n. The counting unit is composed of THn and the lower 5 bits of TLn. The higher 3 bits of TLn are invalid. When the counts of all 13 bits change from 1 to 0, set the TFn overflow flag and reset the initial value
0	1	Mode 1: 16-bit timer/counter n, the counting unit is composed of TLn and THn. When the counts of all 16 bits change from 1 to 0, set the overflow flag TFn and reset the initial value
1	0	Mode 2: 8-bit reload timer/counter n, TLn is used as the counting unit, and THn is used as the reload counting unit. When the counts of all 8 bits change from 1 to 0, set the overflow flag TFn and automatically load the initial value from THn
1	1	Mode 3: For timer/counter 0, it is divided into TL0 and TH0. TL0 is used as an 8-bit timer/counter, which occupies all control bits of Timer0. TH0 is also used as an 8-bit timer, which occupies TR1, TF1 and interrupt resources of Timer1. In this case, Timer1 is still available, but the startup control bit (TR1) and the overflow flag bit (TF1) cannot be used. For timer/counter 1, it stops after it enters mode 3.

Timern count low byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	00h

Timern count high byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	00h

12.2 Timer2

Timer2 is a 16-bit auto reload timer/counter which is configured by T2CON and T2MOD registers, with TH2 as the high byte counter of Timer 2 and TL2 as the low byte counter of Timer2. Timer2 can be used as the baud rate generator of UART0, and it also has the function of 2-channel signal level capture. The capture count is stored in RCAP2 and T2CAP1 registers.

Table 12.2.1 Timer2 registers

Name	Address	Description	Reset value
TH2	CDh	Timer 2 counter high byte	00h
TL2	CCh	Timer 2 counter low byte	00h
T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	00h
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	00h
T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	0000h
RCAP2H	CBh	Count reload/capature 2 data register high byte	00h
RCAP2L	CAh	Count reload/capature 2 data register low byte	00h
RCAP2	CAh	RCAP2L and RCAP2H constitute a 16-bit SFR	0000h
T2MOD	C9h	Timer2 mode register	00h
T2CON	C8h	Timer2 control register	00h

Timer/counter 2 control register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	Timer2 overflow interrupt flag when bT2_CAP1_EN=0 When the Timer2 counts of all 16 bits change from 1 to 0, this overflow flag is set to 1, which requires software to reset. When RCLK=1 or TCLK=1, the bit is not set to 1.	0
7	CAP1F	RW	Timer2 capture 1 interrupt flag when bT2_CAP1_EN=1 It is triggered by the active edge on T2, which requires software to reset.	0
6	EXF2	RW	Timer2 external trigger flag It is triggered by T2EX active edge and set to 1 when EXEN2=1, which requires software to reset.	0

5	RCLK	RW	UART0 receive clock selection 0: Timer1 overflow pulse selected to generate the baud rate. 1: Timer2 overflow pulse selected to generate the baud rate.	0
4	TCLK	RW	UART0 transmit clock selection 0: Timer1 overflow pulse selected to generate the baud rate. 1: Timer2 overflow pulse selected to generate the baud rate.	0
3	EXEN2	RW	T2EX trigger enable bit 0: Ignore T2EX. 1: Reload or capture enabled to be triggered by T2EX active edge	0
2	TR2	RW	Timer2 startup/stop bit Set to 1 to start. Set and cleared by software.	0
1	C_T2	RW	Timer2 clock source selection bit 0: Internal clock selected. 1: Edge count based on falling edge on T2 pin selected.	0
0	CP_RL2	RW	Timer2 function selection bit. This bit should be forced to be 0 if RCLK or TCLK is 1. 0: Timer2 selected as timer/counter to automatically reload the initial value of the count when the counter overflows or T2EX level changes. 1: Timer2 capture 2 function enabled. The active edge on T2EX is captured.	0

Timer/counter 2 mode register (T2MOD):

Bit	Name	Access	Description	Reset value
7	bTMR_CLK	RW	Fastest clock mode enable of T0/T1/T2 timer which has selected fast clock. 1: Fsys without division as the count clock. 0: Divided clock selected. This bit has no effect on the timer that selects the standard clock.	0
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit 0: Standard clock selected. Fsys/12 when in timing/counting mode. Fsys/4 when in UART0 clock mode. 1: Fast clock selected. Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1) when in timing/counting mode. Fsys/2 (bTMR_CLK=0) or Fsys (bTMR_CLK=1) when in UART0 clock mode.	0
5	bT1_CLK	RW	Timer1 internal clock frequency selection bit 0: Standard clock selected, Fsys/12. 1: Fast clock selected. Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1).	0
4	bT0_CLK	RW	Timer0 internal clock frequency selection bit 0: Standard clock selected, Fsys/12.	0

			1: Fast clock selected, Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)		
3	bT2_CAP_M1	RW	Timer2 capture mode high bit	Capture mode selection: X0: From falling ege to falling edge. 01: From any edge to any edge, i.e. level change. 11: From rising edge to rising edge.	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit		0
1	T2OE	RW	Timer2 clock output enable bit 0: Output disabled. 1: T2 pin enabled to output clock. The frequency is the half of the Timer2 overflow rate.		0
0	bT2_CAP1_EN	RW	Capture 1 mode enable when RCLK=0, TCLK=0, CP_RL2=1, C_T2=0 and T2OE=0 1: Capture 1 function enabled. Active edge on T2 is captured. 0: Capture 1 function disabled.		0

Count reload/capature 2 data register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timing/counting mode. High byte of timer captured by CAP2 in capture mode.	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timing/counting mode. Low byte of timer captured by CAP2 in capture mode.	00h

Timer2 counter (T2COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (T2CAP1):

Bit	Name	Access	Description	Reset value
[7:0]	T2CAP1H	RO	High byte of timer captured by CAP1	00h
[7:0]	T2CAP1L	RO	Low byte of timer captured by CAP1	00h

12.3 PWM Register

The PWM_DATA registers in this section are represented in a generic format: a lowercase "n" represents the serial number of ports (n=0～3).

Table 12.3.1 PWMX registers

Name	Address	Description	Reset value
PWM_CK_SE	9Eh	PWM clock setting register	00h

PWM_CTRL	9Dh	PWM control register	02h
PWM_CTRL2	9Fh	PWM extend control register	00h
PWM_DATA0	9Ch	PWM0 data register	00h
PWM_DATA1	9Bh	PWM1 data register	00h
PWM_DATA2	9Ah	PWM2 data register	00h
PWM_DATA3	A3h	PWM3 data register	00h
PWM_CYCLE_L	B6h	PWM cycle register low byte	00h
PWM_CYCLE_H	B7h	PWM cycle register high byte	00h
PWM_CYCLE	B6h	PWM_CYCLE_L and PWM_CYCLE_H constitute a 16-bit SFR.	0000h

PWMn data register (PWM_DATAn):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATAn	RW	In 8-bit or 6-bit data mode, these bits store the current data of PWMn. Duty cycle of PWMn output active level =PWM_DATAn/PWM_CYCLE	00h

In 12-bit data width mode, the low 4 bits in PWM_DATA2 provide PWM0 data high 4 bits. PWM_DATA0 provides PWM0 data low 8 bits. The low 4 bits in PWM_DATA3 provide PWM1 data high 4 bits. PWM_DATA1 provides PWM1 data low 8 bits. The duty cycle of PWM0 output active level =(PWM_DATA2[3:0]*256+PWM_DATA0[7:0])/PWM_CYCLE. PWM1 is similar.

PWM cycle register (PWM_CYCLE):

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0h
[3:0]	PWM_CYCLE_H	RW	Low 4 bits of PWM cycle register high byte. [11:8] of the cycle value.	0h
[7:0]	PWM_CYCLE_L	RW	PWM cycle register low byte.	00h

PWM control register (PWM_CTRL):

Bit	Name	Access	Description	Reset value
7	bPWM_IE_END	RO	PWM cycle period end interrupt enable: 0: PWM cycle period end interrupt disabled. 1: PWM cycle period end interrupt enabled.	0
6	bPWM1_POLAR	RW	PWM1 output polarity control 0: Low level by default, while active high. 1: High level by default, while active low.	0
5	bPWM0_POLAR	RW	PWM0 output polarity control 0: Low level by default, while active high. 1: High level by default, while active low.	0

4	bPWM_IF_END	RW	PWM cycle period end interrupt flag bit 1: A PWM cycle period end interrupt. Write 1 to reset, or reset when the PWM_DATA0 data is reloaded.	0
3	bPWM1_OUT_EN	RW	PWM1 output enable 1: PWM1 output enabled.	0
2	bPWM0_OUT_EN	RW	PWM0 output enable 1: PWM0 output enabled.	0
1	bPWM_CLR_ALL	RW	1: Empty PWM count and FIFO. It requires software to reset.	1
0	Reserved	RO	Reserved	0

PWM extend control register (PWM_CTRL2):

Bit	Name	Access	Description	Reset value
7	bPWM_MOD_12BIT	RW	PWM data width 12-bit mode: 0: 8-bit data mode selected. PWM0~PWM3 support. 1: 12-bit data mode selected. Only for PWM0 and PWM1.	0
6	bPWM_STAG_STAT	RO	PWM staggered output state 0: PWM1/PWM3 is in blanking state. 1: PWM0/PWM2 is in blanking state.	0
5	bPWM2_3_STAG_EN	RW	PWM2/PWM3 staggered output enable: 0: PWM2 and PWM3 output independently; 1: PWM2/PWM3 staggered output (every other cycle)	0
4	bPWM0_1_STAG_EN	RW	PWM0/PWM1 staggered output enable: 0: PWM0 and PWM1 output independently; 1: PWM0/PWM1 staggered output (every other cycle)	0
3	bPWM1_3_DELAY	RW	PWM1/PWM3 delay output mode enable: 0: Output normally. Synchronized with PWM0/PWM2 period. 1: Compared with PWM0/PWM2 period, delay 1 clock output	0
2	Reserved	RO	Reserved	0
1	bPWM3_OUT_EN	RW	PWM3 output enable 1: PWM3 output enabled.	0
0	bPWM2_OUT_EN	RW	PWM2 output enable 1: PWM2 output enabled.	0

PWM clock setting register (PWM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CK_SE	RW	Set PWM clock frequency division factor.	00h

12.4 PWM Function

CH543 and CH541 provide 4-channel 8-bit PWMs or 2-channel 12-bit PWMs. The output duty cycle of PWM can be dynamically modified. After integrating low-pass filtering via simple Resistor-Capacitor (RC), various output voltages can be obtained, which is equivalent to the low-speed Digital-to-Analog Converter (DAC). Among them, PWM0 and PWM1 can also select the reserve polarity output and default output polarity as low level or high level, PWM0 and PWM1 also support 12-bit data width mode.

PWM_CYCLE = PWM_CYCLE_H*256+PWM_CYCLE_L.

In 8-bit data mode, PWMn output duty cycle = PWM_DATAn / PWM_CYCLE.

In 12-bit data mode, PWMn output duty cycle = (PWM_DATA(n+2)[3:0]*256+PWM_DATAn) / PWM_CYCLE.

The duty cycle that is supported ranges from 0% to 100%. If the value of PWM_DATAn is greater than PWM_CYCLE, it is regarded as 100%.

In practical applications, it is recommended to enable the PWM pin output and set the PWM output pin to push-pull output.

12.5 Timer Function

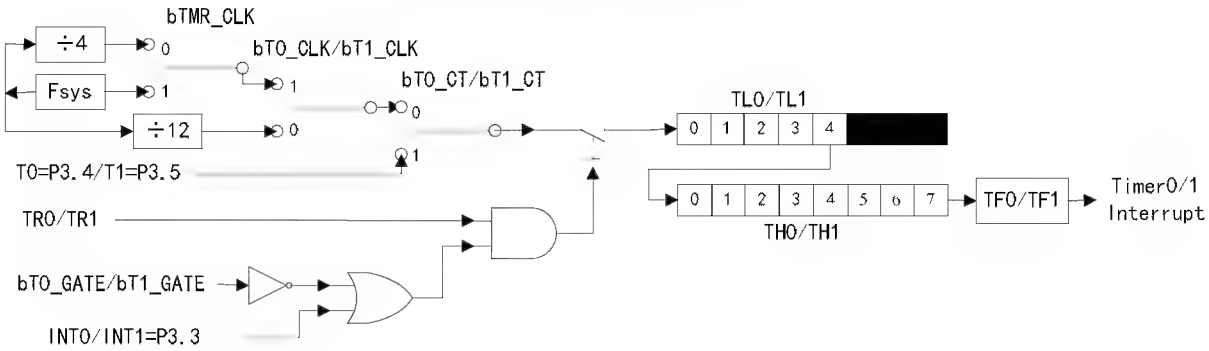
12.5.1 Timer0/1

(1). Set T2MOD to select Timer internal clock frequency. If bTn_CLK(n=0/1) is 0, the corresponding clock of Timer0/1 is Fsys/12. If bTn_CLK is 1, select Fsys/4 or Fsys as the clock based on bTMR_CLK=0 or 1.

(2). Set TMOD to configure the working mode of Timer.

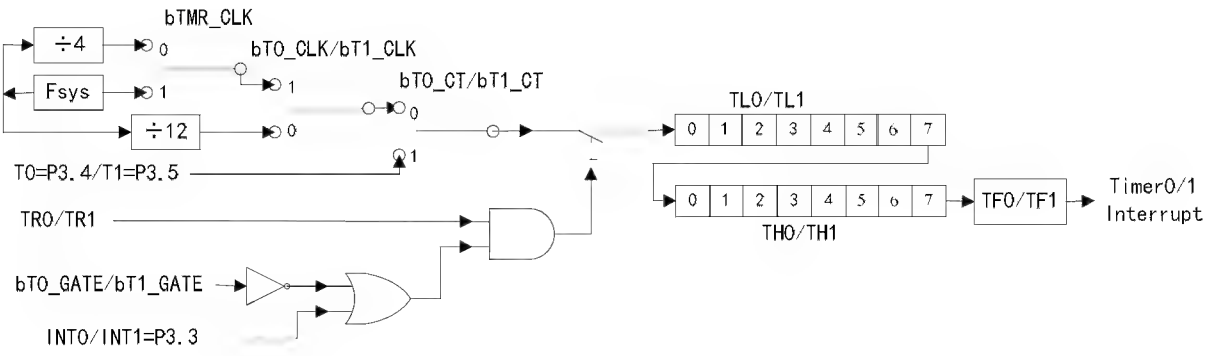
Mode 0: 13-bit timer/counter

Figure 12.5.1.1 Timer0/1 mode 0



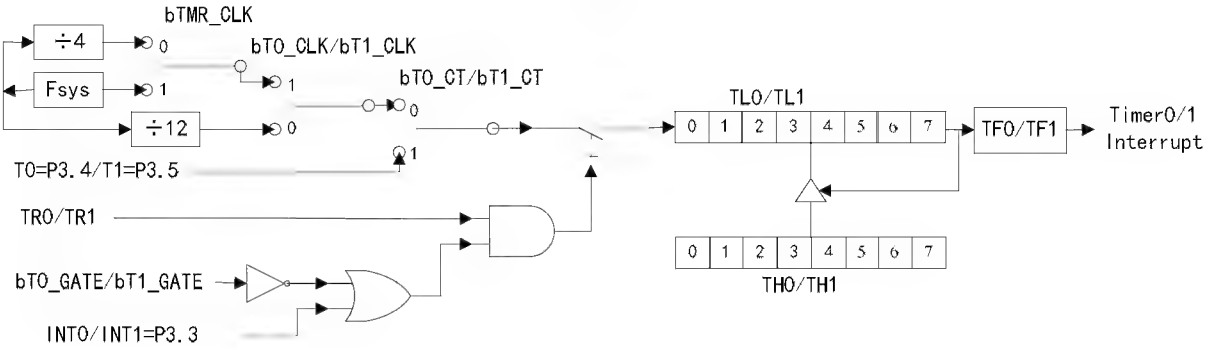
Mode 1: 16-bit timer/counter

Figure 12.5.1.2 Timer0/1 mode 1



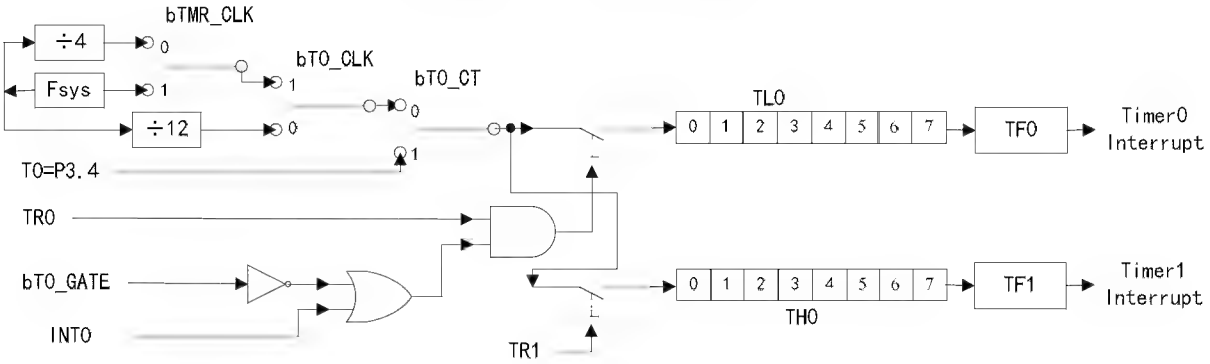
Mode 2: Auto reload 8-bit timer/counter

Figure 12.5.1.3 Timer0/1 mode 2



Mode 3: Timer0 is divided into 2 independent 8-bit timers/counters and borrows the TR1 control bit of Timer1. Timer1 substitutes the borrowed TR1 control bit by whether starting mode 3. Timer 1 stops running when it enters mode 3.

Figure 12.5.1.4 Timer0 mode 3



(3). Set the initial value of TLn and THn(n=0/1).

(4). Set the TRn bit (n=0/1) in TCON to turn on or stop timer/counter, which can be checked by querying the TFn bit (n=0/1) or by interrupt mode.

12.5.2 Timer2

Timer2 16-bit reload timer/counter mode:

(1). Set the RCLK and TCLK bits in T2CON to 0, to select non-UART baud rate generator mode.

(2). Set the C_T2 bit in T2CON to 0, to select the internal clock, and turn to step (3). Alternatively, set to 1 to select the falling edge on T2 pin as the count clock and skip step (3).

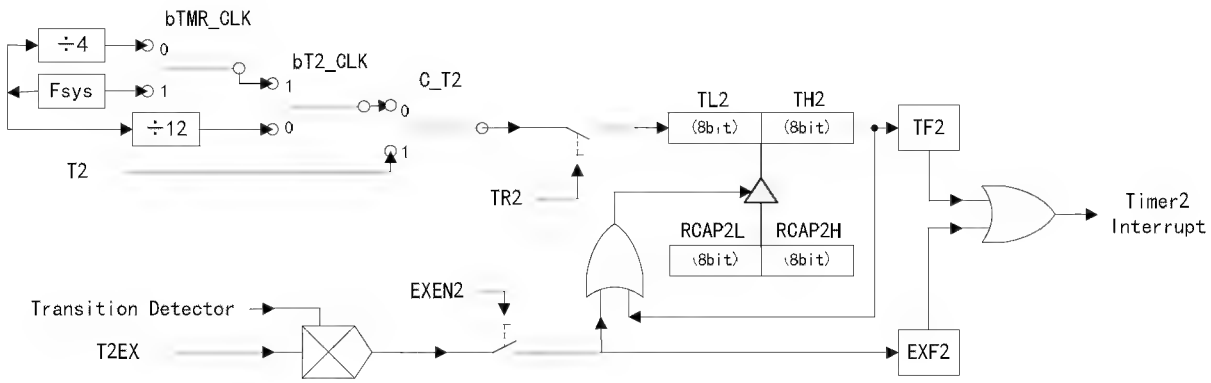
(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, Timer2 clock is Fsys/12. If bT2_CLK is 1, Fsys/4 or Fsys is selected as the clock based on bTMR_CLK=0 or 1.

(4). Set the CP_RL2 bit in T2CON to 0, to select 16-bit reload timer/counter function of Timer2.

(5). Set RCAP2L and RCAP2H as the reload value of timer after overflow. Set TL2 and TH2 as the initial value of the timer (the same as RCAP2L and RCAP2H generally). Set TR2 to 1 to turn on Timer2.

(6). Inquire TF2 or Timer2 interrupt to obtain the current timer/counter state.

Figure 12.5.2.1 Timer2 16-bit reload timer/counter



Timer2 clock output mode:

Refer to the 16-bit reload timer/counter mode and then set the T2OE bit in T2MOD to 1 to enable the TF2 frequency divided by 2 output from T2 pin.

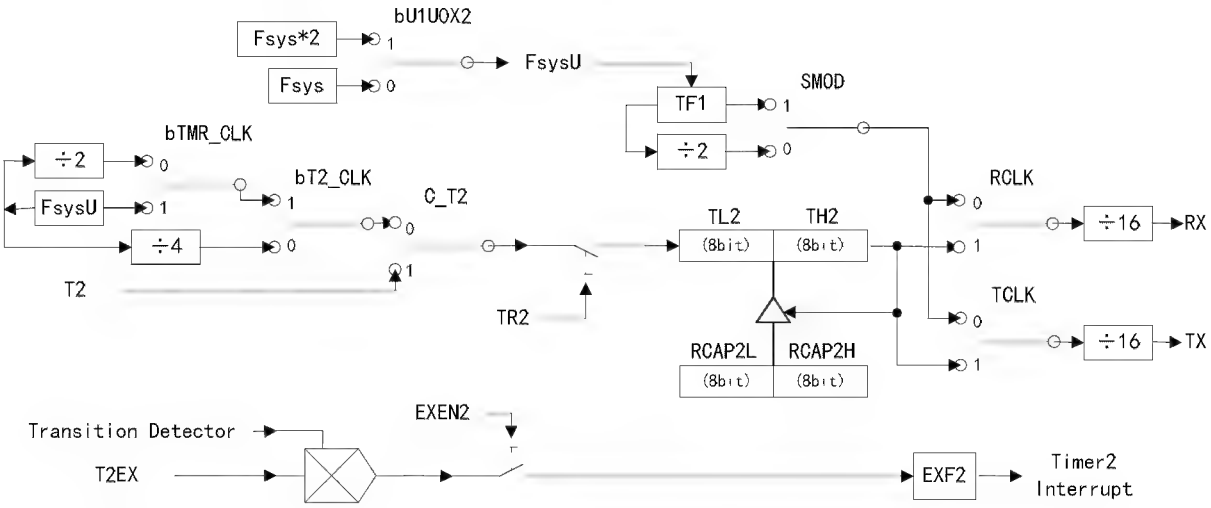
Timer2 UART0 baud rate generator mode:

(1). Set the C_T2 bit in T2CON to 0, to select the internal clock. Alternatively, set to 1 to select the falling edge on T2 pin as the clock. Set the RCLK and TCLK bits in T2CON to 1, or set one of them to 1 as required, to select UART baud rate generator mode.

(2). Set T2MOD to select Timer internal clock frequency. If bT2_CLK is 0, the clock of Timer2 is Fsys/4. If bT2_CLK is 1, select either Fsys/2 or Fsys as the clock based on bTMR_CLK=0 or 1.

(3). Set RCAP2L and RCAP2H as the reload value of timer after overflow. Set TR2 to 1 to turn on Timer2.

Figure 12.5.2.2 Timer2 UART0 baud rate generator



Timer2 signal channel capture mode:

(1). Set the RCLK and TCLK bits in T2CON to 0, to select non-UART baud rate generator mode.

(2). Set the C_T2 bit in T2CON to 0, to select the internal clock, and turn to step (3). Alternatively, set to 1 to select the falling edge on T2 pin as the count clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, Timer2 clock is Fsys/12. If bT2_CLK is 1, either Fsys/4 or Fsys is selected as the clock based on bTMR_CLK=0 or 1.

(4). Set the bT2_CAP_M1 and bT2_CAP_M0 bits in T2MOD, to select corresponding edge capture mode.

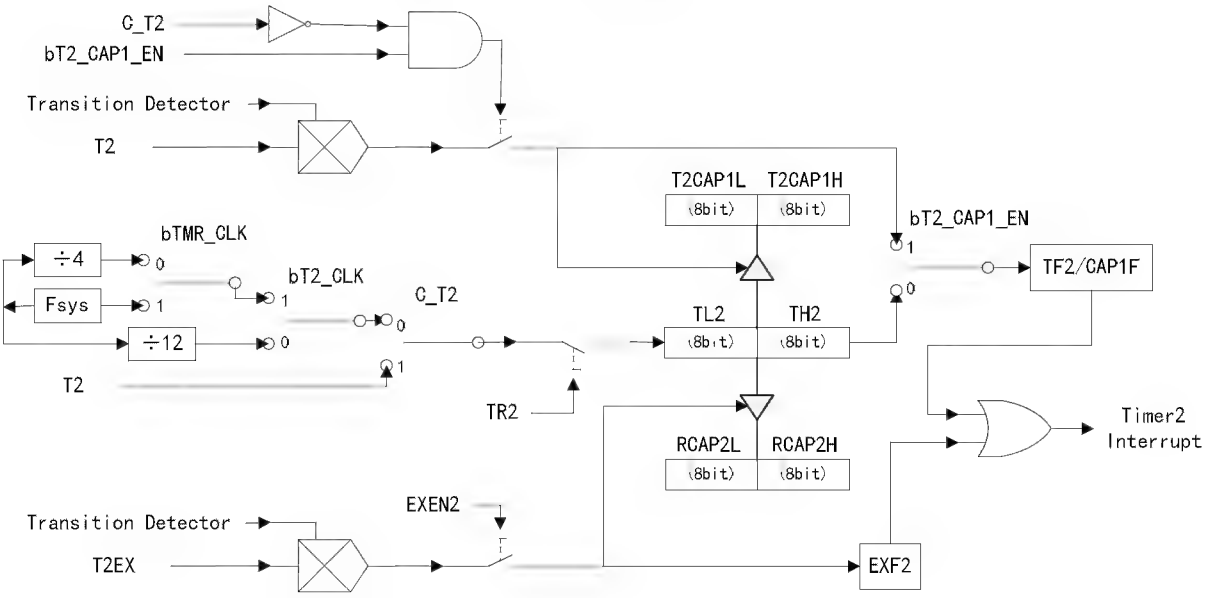
(5). Set the CP_RL2 bit in T2CON to 1, to select the capture function of Timer2 to T2EX pin.

(6). Set TL2 and TH2 as the initial value of the timer, and set TR2 to 1 to turn on Timer2.

(7). When CAP2 capture is completed, RCAP2L and RCAP2H store the current count values of TL2 and TH2 and set EXF2 to generate an interrupt. The difference between the next captured RCAP2L and RCAP2H and the last captured RCAP2L and RCAP2H is the signal width between the two active edges.

(8). If the C_T2 bit in T2CON is 0, and the bT2_CAP1_EN bit in T2MOD is 1, Timer2 is enabled to capture the T2 pin at the same time. When the CAP1 capture is completed, T2CAP1L and T2CAP1H store the current count values of TL2 and TH2, and set CAP1F to generate an interrupt.

Figure 12.5.2.3 Timer2 capture mode



13. Universal Synchronous Receiver Transmitter (UART)

13.1 UART Introduction

CH543 provides a standard MCS51 full-duplex UART, which supports double baud rate. UART data reception/transmission is implemented by physically separated receive/transmit registers via SBUF access. The data written to SBUF is loaded into the transmit register. And the receive buffer register is used for read operation on SBUF.

13.2 UART Register

Table 13.2.1 UART registers

Name	Address	Description	Reset value
SBUF	99h	UART0 data register	xxh
SCON	98h	UART0 control register	00h

UART0 control register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 working mode selection bit 0 0: 8-bit data asynchronous communication selected. 1: 9-bit data asynchronous communication selected.	0
6	SM1	RW	UART0 working mode selection bit 1 0: Fixed baud rate. 1: Variable baud rate, which is generated by timer T1 or T2.	0
5	SM2	RW	UART0 multi-device communication control bit: In mode 2 and mode 3, When SM2=1, If RB8 is 0, RI is not set to 1 and the reception is invalid. If RB8 is 1, RI is set to 1 and the reception is valid. When SM2=0, no matter RB8 is 0 or 1, RI is set when receiving data and the reception is valid. In mode 1, if SM2=1, only when the active stop bit is received can the reception be valid; In mode 0, the SM2 bit must be set to 0.	0
4	REN	RW	UART0 receive enable bit 0: UART0 receive disabled. 1: UART0 receive enabled.	0
3	TB8	RW	The 9th bit of the transmitted data In modes 2 and mode 3, TB8 is used to write the 9th bit of the transmitted data, which can be a parity bit. In multi-device communication, it is used to indicate whether the host sends an address byte or a data byte. Data byte when TB8=0, and address byte when TB8=1.	0
2	RB8	RW	The 9th bit of the received data	0

			In mode 2 and 3, RB8 is used to store the 9th bit of the received data. In mode 1, if SM2=0, RB8 is used to store the received stop bit. In mode 0, RB8 is not used.	
1	TI	RW	Transmit interrupt flag bit Set by hardware at the end of a data byte transmission. It requires software to reset.	0
0	RI	RW	Receive interrupt flag bit Set by hardware at the end of a data byte reception. It requires software to reset.	0

Table 13.2.1.1 UART0 working mode selection

SM0	SM1	Description
0	0	Mode 0, shift register mode. Baud rate is always Fsys/12.
0	1	Mode 1, 8-bit asynchronous communication. Variable baud rate, generated by timer T1 or T2.
1	0	Mode 2, 9-bit asynchronous communication. Baud rate is Fsys/128(SMOD=0) or Fsys/32(SMOD=1)
1	1	Mode 3, 9-bit asynchronous communication. Variable baud rate, generated by timer T1 or T2.

In mode 1 and mode 3, when RCLK=0 and TCLK=0, UART0 baud rate is generated by timer T1. T1 should be set to mode 2 (auto reload 8-bit timer mode). Both bT1_CT and bT1_GATE must be 0. There are the following cases.

Table 13.2.1.2 Formula of UART0 baud rate generated by T1

bTMR_CLK	bT1_CLK	SMOD	bUART_2X	Description
1	1	0	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	0	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	0	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	0	TH1 = 256 - Fsys / 12 / 16 / baud rate
1	1	0	1	TH1 = 256 - Fsys * 2 / 32 / baud rate
1	1	1	1	TH1 = 256 - Fsys * 2 / 16 / baud rate
0	1	0	1	TH1 = 256 - Fsys * 2 / 4 / 32 / baud rate
0	1	1	1	TH1 = 256 - Fsys * 2 / 4 / 16 / baud rate
X	0	0	1	TH1 = 256 - Fsys * 2 / 12 / 32 / baud rate
X	0	1	1	TH1 = 256 - Fsys * 2 / 12 / 16 / baud rate

In mode 1 and mode 3, when RCLK=1 or TCLK=1, UART0 baud rate is generated by timer T2. T2 should be set to 16-bit auto reload baud rate generator mode. Both C_T2 and CP_RL2 must be 0. There are the following cases.

Table 13.2.1.3 Formula of UART0 baud rate generated by T2

bTMR_CLK	bT2_CLK	bUART_2X	Description
1	1	0	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	0	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate
1	1	1	RCAP2 = 65536 - Fsys * 2 / 16 / baud rate
0	1	1	RCAP2 = 65536 - Fsys * 2 / 2 / 16 / baud rate
X	0	1	RCAP2 = 65536 - Fsys * 2 / 4 / 16 / baud rate

UART0 data register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF. The receive register is used to read data from SBUF.	xxh

13.3 UART Applications

(1). Set the MASK_UART_I2C selection pin.

(2). Select UART0 baud rate generator, either from timer T1 or T2, and configure the corresponding counter. Set bTMR_CLK, SMOD and bUART_2X as required.

(3). Turn on T1 or T2.

(4) . Set SM0, SM1, SM2 of SCON to select the working mode of UART0. Set REN to 1 to enable UART0 receiving.

(5). UART interrupt can be set, or R1 and T1 interrupt state can be inquired.

(6). Read/write to SBUF to implement data reception and transmission of UART, and the allowable baud rate error of UART receive signal is not more than 2%.

14. Serial Peripheral Interface (SPI)

14.1 SPI Introduction

CH543 provides one SPI interface for high-speed synchronous data transfer with peripherals.

Features:

(1). Master mode and Slave mode.

(2). Clock mode: mode 0 and mode 3.

(3) Optional, 3-wire full-duplex or 2-wire half-duplex mode.

(4). Optional, MSB-first or LSB-first.

(5). Clock frequency is adjustable, up to half of the system clock frequency.

(6). Built-in 1-byte receive FIFO and 1-byte transmit FIFO.

(7). Supports the first byte pre-load data in slave mode to facilitate the host to obtain the returned data immediately in the first byte.

14.2 SPI Register

Table 14.2.1 SPI registers

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 setup register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data receive/transmit register	xxh
SPI0_STAT	F8h	SPI0 status register	08h

SPI0 setup register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master/slave mode selection bit 0: Master mode. 1: Slave mode/device mode.	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable bit in slave mode 1: FIFO overflow interrupt enabled. 0: FIFO overflow does not generate interrupt.	0
5	bS0_IE_FIRST	RW	Receive first byte completed interrupt enable bit in slave mode 1: Interrupt triggered when the first data byte is received in slave mode. 0: Interrupt is not generated when the first byte is received.	0
4	bS0_IE_BYTE	RW	Data byte transmit completed interrupt enable bit 1: Data byte transmit completed interrupt enabled. 0: Interrupt is not generated when the byte transmission is completed.	0

3	bS0_BIT_ORDER	RW	Order control bit of data byte 0: MSB first. 1: LSB first.	0
2	Reserved	RO	Reserved	0
1	bS0_SLV_SELT	RO	Chip select activate status bit in slave mode 0: Not selected currently. 1: Being selected currently	0
0	bS0_SLV_PRELOAD	RO	Pre-load data status bit in slave mode 1: Current pre-load state after valid chip select and before the data is not transmitted	0

SPI0 clock setting register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	Set SPI0 clock frequency division factor in master mode.	20h

SPI0 preset data register in slave mode (SPI0_S_PRE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Preload first transmitted data in slave mode.	20h

SPI0 control register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	SPI0 MISO output enable 1: SPI0 MISO output enabled. 0: SPI0 MISO output disabled.	0
6	bS0_MOSI_OE	RW	SPI0 MOSI output enable 1 SPI0 MOSI output enabled. 0: SPI0 MOSI output disabled.	0
5	bS0_SCK_OE	RW	SPI0 SCK output enable 1: SPI0 SCK output enabled. 0: SPI0 SCK output disabled.	0
4	bS0_DATA_DIR	RW	SPI0 data direction control bit 0: Output. Only writing to FIFO is regarded as an effective operation, and an SPI transmission is started. 1: Input. Reading/writing to FIFO is regarded as an effective operation, and an SPI transmission is started.	0
3	bS0_MST_CLK	RW	SPI0 master clock mode control bit 0: Mode 0. SCK defaults to low level when free. 1: Mode 3. SCK defaults to high level.	0
2	bS0_2_WIRE	RW	2-wire half-duplex mode enable bit of SPI0 0: 3-wire full-duplex mode (SCK, MOSI and MISO). 1: 2-wire half-duplex mode (SCK, MISO).	0
1	bS0_CLR_ALL	RW	1: Empty SPI0 interrupt flag and FIFO.	1

			It requires software to reset.	
0	bS0_AUTO_IF	RW	Enable bit that allows automatic clear of byte receive completed interrupt flag through FIFO effective operation 1: Auto clear the byte receive completed interrupt flag (S0_IF_BYTE) during effective read/write operation on FIFO.	0

SPI0 data receive/transmit register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Including the transmit FIFO and the receive FIFO which are physically separated. The receive FIFO is used for read operation. And the transmit FIFO is used for write operation. Effective read/write operation can initiate an SPI transmission.	xxh

SPI0 status register (SPI0_STAT):

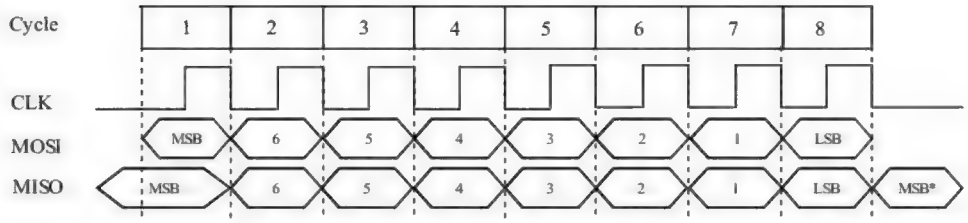
Bit	Name	Access	Description	Reset value
7	S0_FST_ACT	RO	1: Currently, reception of the first byte is completed in slave mode.	0
6	S0_IF_OV	RW	FIFO overflow flag bit in slave mode 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. When bS0_DATA_DIR=0, transmit FIFO empty triggers interrupt. When bS0_DATA_DIR=1, receive FIFO full triggers interrupt.	0
5	S0_IF_FIRST	RW	First byte receive completed interrupt flag bit in slave mode 1: The first byte is received. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	S0_IF_BYTE	RW	Data byte transmit completed interrupt flag bit 1: One byte transmission is completed. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset, or reset by FIFO effective operation when bS0_AUTO_IF=1.	0
3	S0_FREE	RO	SPI0 free flag bit 1: No SPI shift at present, usually it is in the free period between the data bytes	1
2	S0_T_FIFO	RO	SPI0 transmit FIFO count. 0 and 1 both are valid.	0
1	Reserved	RO	Reserved	0
0	S0_R_FIFO	RO	SPI0 receive FIFO count. 0 and 1 both are valid.	0

14.3 SPI Transfer Format

SPI master mode supports 2 transfer formats, i.e. mode 0 and mode 3, which can be selected by setting the bSn_MST_CLK bit in SPI control register (SPIn_CTRL). CH543 always samples MISO data on the rising edge of CLK. The data transfer formats are shown in the figures below.

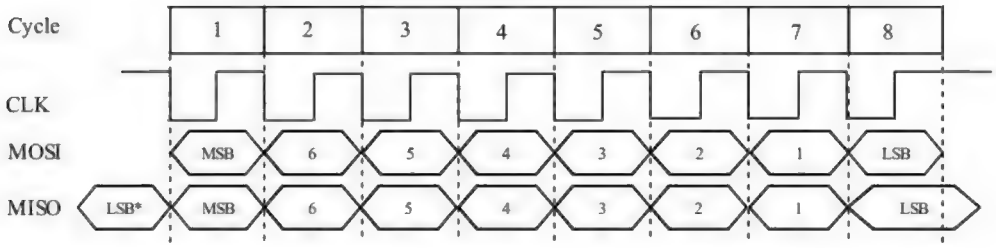
Mode 0: bSn_MST_CLK = 0

Figure 14.3.1 SPI mode 0 timing diagram



Mode 3: bSn_MST_CLK = 1

Figure 14.3.2 SPI mode 3 timing diagram



14.4 SPI Configuration

14.4.1 Master Mode

In SPI master mode, SCK pin outputs serial clock, and the chip select output pin can be specified as any I/O pin.

SPI0 configuration procedure:

(1) Set the SPI clock setting register (SPI0_CK_SE) to configure SPI clock frequency.

(2). Set the bS0_MODE_SLV bit in the SPI setup register (SPI0_SETUP) to 0, to select Master mode.

(3). Set the bS0_MST_CLK bit in the SPI control register (SPI0_CTRL) to select mode 0 or mode 3 as required.

(4). Set the bS0_SCK_OE and bS0_MOSI_OE bits in the SPI control register (SPI0_CTRL) to 1, and set the bS0_MISO_OE bit to 0, to set the P1 port direction bSCK and bMOSI to output, bMISO to input, and chip select pin to output.

Data transmission:

(1). Write to the SPI0_DATA register, write data to FIFO to automatically initiate an SPI transfer.

(2). Wait for S0_FREE to be 1, it indicates that the transmission is completed and the transmission of the next byte can be proceeded.

Data reception:

(1). Write to the SPI0_DATA register, write any data to FIFO, e.g. 0FFh to initiate an SPI transfer.

(2). Wait for S0_FREE to be 1, it indicates that the reception is completed and SPI0_DATA can be read to

obtain the received data.

(3). If bS0_DATA_DIR is set to 1 previously, the above read operation still can initiate the next SPI transfer, otherwise it will not start.

14.4.2 Slave Mode

Only SPI0 supports Slave mode. In Slave mode, SCK pin is used to receive the serial clock of the connected SPI host.

(1). Set the bS0_MODE_SLV bit in the SPI0 setup register (SPI0_SETUP) to 1, to select Slave mode.

(2). Set the bS0_SCK_OE and bS0_MOSI_OE bits in the SPI0 control register (SPI0_CTRL) to 0, and set the bS0_MISO_OE bit to 1, to set the P1 port direction bSCK, bMOSI, bMISO and chip select pin to input. When SCS is active (low level), MISO output is automatically enabled. In this case, it is recommended to set MISO pin to high impedance input (P1_MOD_OC[6]=0, P1_DIR_PU[6]=0), so that MISO does not output during invalid chip select, which is convenient for sharing SPI bus.

(3). Optionally, set the preset data register in SPI slave mode (SPI0_S_PRE), to be automatically loaded into the buffer for the first time after chip select for external output. After 8 serial clocks, that is, the first byte data transfer and exchange is completed, CH543 obtains the first byte of data (possibly command code) sent by the external SPI host, and the external SPI host obtains the preset data (possibly the status value) in SPI0_S_PRE through exchange. The bit7 in the SPI0_S_PRE register is automatically loaded into the MISO pin during the low level period of SCK after the SPI chip select is valid. For SPI mode 0, if the bit7 in SPI0_S_PRE is preset by CH543, the external SPI host obtains the preset value of bit7 in SPI0_S_PRE by inquiring the MISO pins when the SPI chip select is valid but there is no data transfer, thereby the value of bit7 in SPI0_S_PRE can be obtained only by the valid SPI chip select.

Data transmission:

Inquire S0_IF_BYTE or wait for interrupt. After each SPI data byte transfer, write to the SPI0_DATA register, and write the data to be sent to FIFO. Or wait for S0_FREE to be changed from 0 to 1, and the transmission of the next byte can be proceeded.

Data reception:

Inquire S0_IF_BYTE or wait for interrupt. After each SPI data byte transfer, read the SPI0_DATA register to obtain the received data from FIFO. Inquire S0_R_FIFO to know whether there are remaining bytes in FIFO.

15. ADC, TKEY, CMP and ISINK

15.1 ADC/TKEY/CMP/ISINK Introduction

The signal chain analogue modules of the CH543 chip include: 12-bit analogue-to-digital converter ADC, capacitive touch key charging and discharging module TKEY, voltage comparator CMP/buffer BUF module, programmable fill current ISINK. The CH541 does not support the ISINK module.

The ADC has 12 external analog signal input channels and 2 internal input channels. It supports time-sharing acquisition and supports analog input voltage which ranges from 0 to VDD. P1.0/P1.1/RST only supports analog input voltage which ranges from 0 to (VDD-0.6V). When bRST_VOL_SEL=1, RST supports the voltage which ranges from 0 to (4*VDD-2.4V). Except RST, other external channels all support capacitive touch-key detection.

3 optional applications of CMP/ BUF:

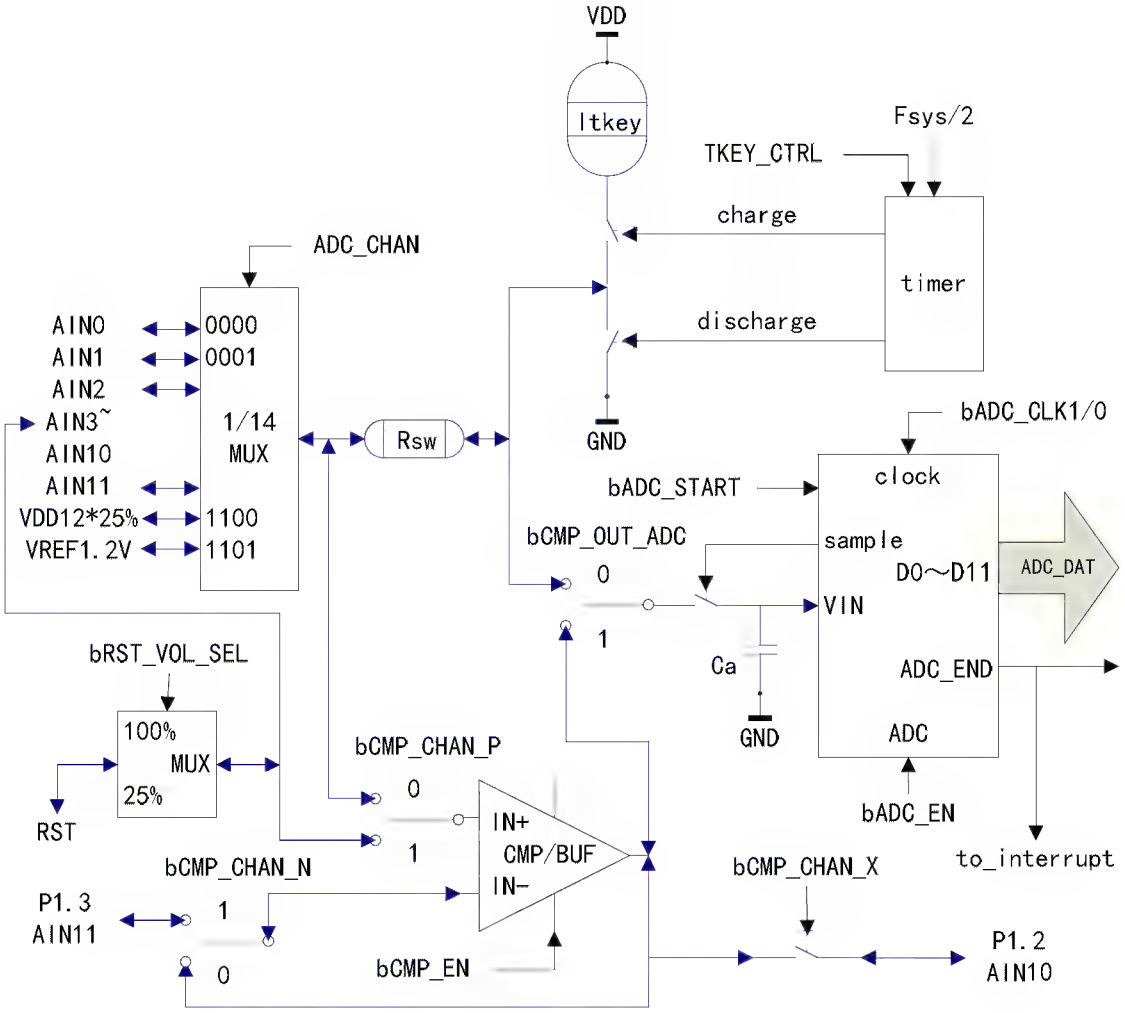
(1). Used for ADC signal input buffer, to support high-impendance signal source fast sample and ADC.

(2). Simply amplify the input analog signal and output it to P1.2 and optionally transmit it to the ADC. 2 external resistors are required to be connected to set the gain.

(3). Compare the voltage of the input analog signal with the voltage of P1.3 input analog signal, and output the result to P1.2/INT0_.

The programmable sink current ISINK is used to draw current from external sources, with a total of 9-bit data width, 512 steps of current, in steps of approximately 0.465 uA. If this current is applied to an external 43 KΩ resistor in series, it produces a programmable voltage in steps of 20 mV, equivalent to a 9-bit DAC.

Figure 15.1.1 ADC/TKEY/CMP structure diagram (blue lines represent analog signals)



15.2 ADC Register

Table 15.2.1 ADC registers

Name	Address	Description	Reset value
ADC_CTRL	F3h	ADC control and status register	00h
ADC_DAT_H	F5h	ADC result data high byte (read only)	0xh
ADC_DAT_L	F4h	ADC result data low byte (read only)	xxh
ADC_DAT	F4h	ADC_DAT_L and ADC_DAT_H constitute a 16-bit SFR	0xxxh
ADC_CHAN	F6h	ADC analog signal channel selection register	00h

ADC control and status register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
7	bTKEY_ACT	RO	Touch-key detection activity 1: The capacitor is being charged and the ADC is being measured.	0

6	Reserved	RO	Reserved	0
5	bADC_IF	RW	ADC conversion completed interrupt flag 1: An ADC conversion is completed. Write 1 to reset, or write to ADC_CHAN to reset, or write to TKEY_CTRL to reset.	0
4	bADC_START	RW	ADC startup control bit Set to 1 to start an ADC conversion. The bit is reset automatically after the ADC conversion is completed	0
3	bADC_EN	RW	ADC power enable bit 0: ADC power supply OFF. It enters the sleep state. 1: ADC power supply ON.	0
2	Reserved	RO	Reserved	0
1	bADC_CLK1	RW	ADC reference clock frequency selection high bit	0
0	bADC_CLK0	RW	ADC reference clock frequency selection low bit	0

Table 15.2.2 ADC reference clock frequency selection table

bADC_CLK1	bADC_CLK0	ADC reference clock frequency	Time required to complete an ADC	Applicable scope
0	0	750KHz	1024 Fosc cycles	Rs<=20KΩ or Cs>=0.08uF
0	1	1.5MHz	512 Fosc cycles	Rs<=10KΩ or Cs>=0.08uF
1	0	3MHz	256 Fosc cycles	Rs<=5KΩ or Cs>=0.08uF
1	1	6MHz	128 Fosc cycles	Rs<=2KΩ or Cs>=0.08uF

Note: The sampling time is 4 reference clocks. Cs refers to capacitance in parallel to signal source. Rs refers to internal resistance in series with signal source.

For RST and 2 internal ADC channels, the internal resistance is large, and a smaller reference clock needs to be selected, or sample more times and discard the previous values.

When P1.0/P1.1 input analog voltage is high and close to VDD, a smaller reference clock needs to be selected, or sample more times.

ADC analog signal channel selection register (ADC_CHAN):

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0000b
[3:0]	MASK_ADC_CHAN	RW	When bADC_EN=1, select the signal source of the analog signal channel. When bADC_EN=0, the analog signal channel is closed.	0000b

Table 15.2.3 CMP positive input and ADC/TKEY input external channel selection table

bADC_EN	ADC_CHAN	Select the signal source of the analog signal channel
0	xxxxb	Disconnect the internal and external signal channels (AIN0~AIN11). Suspended.
1	0000b	Connect to external signal: AIN0 (P1.0)
1	0001b	Connect to external signal: AIN1 (P1.1)

1	0010b	Connect to external signal: AIN2 (P3.2)
1	0011b	Connect to external signal: AIN3 (25% of RST or RST). TKEY does not support.
1	0100b	Connect to external signal: AIN4 (P1.4)
1	0101b	Connect to external signal: AIN5 (P1.5)
1	0110b	Connect to external signal: AIN6 (P1.6)
1	0111b	Connect to external signal: AIN7 (P1.7)
1	1000b	Connect to external signal: AIN8 (P3.6)
1	1001b	Connect to external signal: AIN9 (P3.7)
1	1010b	Connect to external signal: AIN10 (P1.2)
1	1011b	Connect to external signal: AIN11 (P1.3)
1	1100b	Connect to internal power supply: 25% of VDD12
1	1101b	Connect to internal reference voltage: about 1.2V VREF12, there may be noise.

ADC data register (ADC_DAT):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DAT_H	RO	High byte of ADC sampling result data	0xh
[7:0]	ADC_DAT_L	RO	Low byte of ADC sampling result data	xxh

15.3 TKEY Register

Table 15.3.1 TKEY register

Name	Address	Description	Reset value
TKEY_CTRL	F2h	Touch-key charging pulse width control register (write only)	00h

Touch-key charging pulse width control register (TKEY_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	TKEY_CTRL	WO	Touch key charging pulse width value Only the lower 7 bits are valid. Count in the unit of (2/Fsys). It automatically initates ADC to measure the voltage on the capacitor when the timing is up.	00h

15.4 CMP Register

Table 15.4.1 CMP and BUF register

Name	Address	Description	Reset value
ANA_CTRL	F1h	Analog CMP control register	00h

Analog CMP control register (ANA_CTRL):

Bit	Name	Access	Description	Reset value
7	bCMP_CHAN_X	RW	Analog CMP output CO enable: 0: Analog CMP output disabled. 1: Output the result to P1.2.	0
6	bCMP_OUT_ADC	RW	ADC sample input signal source selection: 0: Switch to the analog channel selected by ADC_CHAN and input directly. 1: Switch to analog signal after bufferred or amplified by CMP.	0
5	bCMP_CHAN_N	RW	Analog CMP signal- CM selection: 0: Switch to CMP output, as the signal buffer. 1: Switch to P1.3.	0
4	bCMP_CHAN_P	RW	Analog CMP signal+ CP selection: 0: Switch to the analog channel selected by ADC_CHAN. 1: Switch to the RST pin. Voltage controlled by bRST_VOL_SEL.	0
3	bCMP_EN	RW	CMP power control bit: 0: CMP power OFF. Enter sleep state. 1: CMP power ON.	0
2	bCMP_IE	RW	CMP result changed interrupt enable bit: 1: CMP result changed interrupt enabled. 0: CMP result changed interrupt disabled.	0
1	bCMP_IF	RW	CMP result changed interrupt flag: 1: CMP result changed at least once. Write 1 to reset, or reset automatically when it enters corresponding interrupt service program.	0
0			Reserved	0

15.5 ISINK Register

Table 15.5.1 ISINK register

Name	Address	Description	Reset value
ISINK_DATA	AEh	Programmable sink current ISINK high 8-bit data register	00h
ISINK_LSB	AFh	Programmable sink current ISINK preset lowest bit register (write only)	00h
ISINK_LSB	AFh	Programmable sink current ISINK current lowest bit	00h

		register (read-only)	

Programmable sink current ISINK data registers (ISINK_DATA, ISINK_LSB), ISINK_DATA is writable in safe mode only.

Bit	Name	Access	Description	Reset value
[7:1]	Reserved	RO	Reserved	00h
0	ISINK_LSB	WO	The lowest bit of the preset programmable sink current data to be validated.	0
0	ISINK_LSB	RO	The lowest bit of the 9-bit programmable sink current data currently in effect	0
[7:0]	ISINK_DATA	RW	The high 8 bits of programmable sink current data. The lowest bit is preset first, then the high 8 bits of data are written, and the hardware automatically writes the preset bits to the 9-bit width programmable sink current data synchronously. The programmable sink current module ISINK is turned off when all 9 bits of data are 0.	00h

15.6 ADC and Touch-Key Functions

ADC sampling mode configuration procedure:

(1). Set the bADC_EN bit in ADC_CTRL to 1, to enable ADC module, and set the bADC_CLK0/1 to select frequency.

(2). Set the ADC_CHAN register to select external signal channel or internal signal channel.

(3). Optional, clear the bADC_IF interrupt flag. Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(4). Set bADC_START in ADC_CTRL register to start an ADC conversion.

(5). Wait for bADC_START to be changed into 0, or wait for bADC_IF to be set to 1 (if reset before), it indicates that ADC conversion is completed and the result data can be read through ADC_DAT. This data is the value of the input voltage relative to 4095 equal parts of the VDD supply voltage, for example, if the result data is 475, it indicates that the input voltage is approximate to 475/4095 of the VDD voltage. If the VDD supply voltage is also uncertain, another determined reference voltage value can be measured, and the measured input voltage value and the VDD supply voltage value can be calculated proportionally.

(6). If bADC_START is set again, the next ADC conversion can be started.

(7). If the ADC reference clock frequency is high and it results in a short sampling time or high internal resistance of signal source in series, or large Rsw internal resistance due to the low supply voltage, then it is possible that Ca could not sample enough signal voltage and affect the ADC result. The solution is to discard the first ADC data, immediately start the second ADC and use its ADC result data, namely sample twice.

(8). In case of high accuracy requirement, it is recommended to calibrate before use and eliminate the inherent deviation with software.

Touch-Key detection procedure:

(1). Set the bADC_EN bit in ADC_CTRL register to 1, to enable ADC module, and set the bADC_CLK0/1

to select frequency.

(2). Set the ADC_CHAN register to select touch key signal channel.

(3). Select the appropriate charging pulse width according to the actual capacitance of the touch key, and write into the TKEY_CTRL register. The simple calculation formula is as follows (assume that: the external capacitance of the touch key Ckey=25pF, VDD=3.3V, Fsys=12MHz, rough calculation):

count=(Ckey+Cint)*0.7VDD/ITKEY/(2/Fsys)=(25p+15p)*0.35*3.3*12M/50u=11

TKEY_CTRL=count > 127 ? 127 : count

(4). Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(5). When the capacitor charge timing of the touch key is reached, CH543 automatically sets bADC_START to start ADC to measure the voltage on the capacitor

(6). Wait for bTKEY_ACT to be changed into 0, or wait for bADC_IF to be set to 1, it indicates the completion of charging and ADC conversion and the result data can be read through ADC_DAT. The software then compares this value with that without any key, and determines whether the touch key is pressed or not according to the change in capacitance.

(7). Shift to step (2) as required and select another touch key signal channel for detection.

For the above selected external analog signal channel, the GPIO pin where it's located must be set in either high-impedance input mode or open-drain output mode and in output 1 state (equivalent to high-impedance input), Pn_DIR_PU[x]=0, and turn off the pull-up resistor and pull-down resistor.

16. USB Controller

16.1 Introduction

CH543 is integrated with a USB host controller which supports full-speed (12Mbps) and low-speed (1.5Mbps) USB transfer. It is integrated with a USB device controller, which supports full speed and low speed, and supports up to 64 bytes of data packet.

Main features of CH543 USB controllers:
(1). Support USB Host function and USB Device function. For CH541, only USB Device is supported.
(2). USB 2.0 full-speed (12Mbps) and low-speed (1.5Mbps) transfer.
(3). USB control transfer, bulk transfer, interrupt transfer, synchronous/simultaneous transfer.
(4). Up to 64 bytes of data packet. Built-in FIFO. Support interrupts and DMA.

CH543 USB registers are divided into 3 categorys. Some of them are multiplexed in Host and Device modes.
(1). USB global registers.
(2). USB device controller registers.
(3). USB host controller and root-hub registers.

16.2 Global Register

Table 16.2.1 USB global registers (That marked in grey is controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
USB_PULL	B4h	USB port pull-up/pull-down resistor/current control register	0001 0001b
USB_INT_FG	D8h	USB interrupt flag register	0000 0000b
USB_INT_ST	D9h	USB interrupt status register (read only)	0011 xxxxb
USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
USB_RX_LEN	DBh	USB reception length register (read only)	0xxx xxxxb
USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB port pull-up/pull-down resistor/current control register (USB_PULL):

Bit	Name	Access	Description	Reset value
7	bUDM_PUE	RW	USB DM pin internal 1.5KΩ pull-up resistor enable: 1: USB DM pin internal 1.5KΩ pull-up resistor enabled. 0: USB DM pin internal 1.5KΩ pull-up resistor disabled.	0
6	bUDM_PDE	RW	USB DM pin internal 16KΩ pull-down resistor enable: 1: USB DM pin internal 16KΩ pull-down resistor enabled. 0: USB DM pin internal 16KΩ pull-down resistor disabled.	0
5	bUDM_PCS1	RW	MASK_UDM_PCS used to configure the internal pull-up/pull-down current on DM pin:	0

4	bUDM_PCS0	RW	00: The pull-up/pull-down current disabled. 01: Weak pull-down current enabled, about 2uA. Recommended to be mutually exclusive with bUDM_PUE. 10: Weak pull-up current enabled, about 10uA. Recommended to be mutually exclusive with bUDM_PDE. 11: Pull-down current enabled, about 100uA. Recommended to be mutually exclusive with bUDM_PUE.	1
3	bUDP_PUE	RW	USB DP pin internal 1.5KΩ pull-up resistor enable: 1: USB DP pin internal 1.5KΩ pull-up resistor enabled. 0: USB DP pin internal 1.5KΩ pull-up resistor disabled. If bUDP_PUE=1 and MASK_UDP_PCS=10, an additional diode is connected, for VDD>=4.5V (example: during 5V sleep).	0
2	bUDP_PDE	RW	USB DP pin internal 16KΩ pull-down resistor enable: 1: USB DP pin internal 16KΩ pull-down resistor enabled. 0: USB DP pin internal 16KΩ pull-down resistor disabled.	0
1	bUDP_PCS1	RW	MASK_UDP_PCS used to configure the internal pull-up/pull-down current on DP pin: 00: The pull-up/pull-down current disabled. 01: Weak pull-down current enabled, about 2uA. Recommended to be mutually exclusive with bUDP_PUE. 10: Weak pull-up current enabled, about 10uA. Recommended to be mutually exclusive with bUDP_PDE. 11: Pull-down current enabled, about 100uA. Recommended to be mutually exclusive with bUDP_PUE.	0
0	bUDP_PCS0	RW		1

USB interrupt flag register (USB_INT_FG):

Bit	Name	Access	Description	Reset value
7	U_IS_NAK	RO	In USB device mode, 1: NAK busy response is received during current USB transfer. 0: Non-NAK response is received	0
6	U_TOG_OK	RO	Current USB transmission DATA0/1 synchronization flag matching state 1: Synchronization and the data is valid. 0: Desynchrony and the data may be invalid	0
5	U_SETUP_ACT	RO	In USB device mode, if this bit is 1, 8-byte SETUP request packet has been received successfully. The SETUP token does not affect bUIS_TOG_OK, bUIS_TOKEN1/0, MASK_UIS_ENDP or USB_RX_LEN.	0
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag bit 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the	0

			corresponding bit in the register.	
3	UIF_HST_SOF	RW	SOF timing interrupt flag bit in USB host mode 1: SOF timing interrupt, triggered by SOF packet transfer completion. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
2	UIF_SUSPEND	RW	USB bus suspend/wakeup event interrupt flag bit 1: There is an interrupt, triggered by USB suspend event or wakeup event. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
1	UIF_TRANSFER	RW	USB transfer completed interrupt flag bit 1: There is an interrupt, triggered by a USB transfer completion. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
0	UIF_DETECT	RW	USB device connection or disconnection event interrupt flag bit in USB host mode 1: There is an interrupt, triggered by detecting a USB device connection or disconnection. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag bit in USB device mode 1: There is an interrupt, triggered by USB bus reset event. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0

USB interrupt status register (USB_INT_ST):

Bit	Name	Access	Description	Reset value
7	bUIS_SETUP_ACT	RO	In the USB device mode, when this bit is 1, 8-byte SETUP request packet has been successfully received. The same as U_SETUP_ACT.	0
6	bUIS_TOG_OK	RO	Current USB transmission DATA0/1 synchronization flag matching state 1: Synchronization. 0: Desynchrony. The same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	The token PID high bit of the current USB transfer service in device mode	1

4	bUIS_TOKEN0	RO	The token PID low bit of the current USB transfer service in device mode	1
[3:0]	MASK_UIS_ENDP	RO	The endpoint serial number of the current USB transfer service in USB device mode 0000: Endpoint 0. ... 1111: Endpoint 15.	xxxxb
[3:0]	MASK_UIS_H_RES	RO	The response PID of the current USB transfer service in USB host mode, 0000: Device has no response or timeout. Other values: Response PID	xxxxb

BUIS_TOKEN1 and bUIS_TOKEN0 constitute MASK_UIS_TOKEN, which is used to identify the token PID of the current USB transfer service in USB device mode. 00: OUT packet. 01: SOF packet. 10: IN packet. 11: Free.

When MASK_UIS_TOKEN is not free and bUIS_SETUP_ACT is 1, it is required to process the former first, clear UIF_TRANSFER after the former is processed to make the former enter free state, and then process the latter, and finally clear UIF_TRANSFER again.

USB miscellaneous status register (USB_MIS_ST):

Bit	Name	Access	Description	Reset value
7	bUMS_SOF_PRES	RO	SOF packet predictive status bit in USB host mode. If this bit is 1, SOF packet is to be sent, and it is automatically delayed if there are other USB data packets.	x
6	bUMS_SOF_ACT	RO	SOF packet transfer status in USB host mode 1: SOF packet is being transmitted. 0: The transmission is completed, or idle.	x
5	bUMS_SIE_FREE	RO	Free status bit of USB protocol processor 0: Busy, and USB transfer is in progress. 1: USB in idle.	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready status bit 0: Receive FIFO is null. 1: Receive FIFO is not null	0
3	bUMS_BUS_RESET	RO	USB bus reset status bit 0: No USB bus reset at present. 1: USB bus reset is in progress.	1
2	bUMS_SUSPEND	RO	USB suspend status bit 0: There is USB activity at present. 1: There has been no USB activity for some time, request to be suspended.	0
1	bUMS_DM_LEVEL	RO	In USB host mode, record the state of DM pin when the USB device is just connected to the hub0 port 0: Low level.	0

			1: High level. Used to judge full speed or low speed	
0	bUMS_DEV_ATTACH	RO	USB port USB device connection state bit in USB host mode 1: USB port has been connected to the USB device. 0: USB port is not connected to the USB device.	0

USB reception length register (USB_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes of the data received by the USB endpoint currently.	xxh

USB interrupt enable register (USB_INT_EN):

Bit	Name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	1: Receive SOF packet interrupt in USB device mode enabled. 0: Receive SOF packet interrupt in USB device mode disabled.	0
6	bUIE_DEV_NAK	RW	1: Receive NAK interrupt in USB device mode enabled. 0: Receive NAK interrupt in USB device mode disabled.	0
5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	1: FIFO overflow interrupt enabled. 0: FIFO overflow interrupt disabled.	0
3	bUIE_HST_SOF	RW	1: SOF timing interrupt in USB host mode enabled. 0: SOF timing interrupt in USB host mode disabled.	0
2	bUIE_SUSPEND	RW	1: USB bus suspend/wakeup event interrupt enabled. 0: USB bus suspend/wakeup event interrupt disabled.	0
1	bUIE_TRANSFER	RW	1: USB transfer completed interrupt enabled. 0: USB transfer completed interrupt disabled.	0
0	bUIE_DETECT	RW	1: USB device connection/disconnection event interrupt in USB host mode enabled. 0: USB device connection/disconnection event interrupt in USB host mode disabled.	0
0	bUIE_BUS_RST	RW	1: USB bus reset event interrupt in USB device mode enabled. 0: USB bus reset event interrupt in USB device mode disabled.	0

P3.6/P3.7 level change interrupt:

When bUC_CLR_ALL=1, bUIE_TRANSFER=0, bUC_HOST_MODE=0, bUC_DEV_SWAP=0, and bUC_DEV_EN=0 (default state after reset), DP/DM is disabled, and GPIO is enabled. For P3.6 or P3.7 in high-impendance input mode, this GPIO level change interrupt function is enabled automatically, that is, if P3_MOD_OC[6]=0 and P3_DIR_PU[6]=0, USB interrupt is generated when P3.6 pin input state is different from the value in P3.6 output register. The interrupt request is cancelled after updating the value

in the output register with the new state of the P3.6 pin. P3.7 is similar to is. In addition, P3.6 and P3.7 level change interrupts can be enabled.

USB control register (USB_CTRL):

Bit	Name	Access	Description	Reset value
7	bUC_HOST_MODE	RW	USB working mode selection bit 0: USB device mode selected. 1: USB host mode selected.	0
6	bUC_LOW_SPEED	RW	USB bus signal transfer rate selection bit 0: Full speed, 12Mbps. 1: Low speed, 1.5Mbps.	0
5	bUC_DEV_SWAP	RW	DP/DM swap enable in USB device mode 0: DP/DM swap disabled. 1: DP and DM USB full-speed signal pins swapped when bUD_LOW_SPEED=1 and bUC_LOW_SPEED=0.	0
4	bUC_DEV_EN	RW	USB device enable in USB device mode 1: USB device transfer enabled. It is required that internal pull-up resistor or external resistor is enabled by USB_PULL firstly.	0
5	bUC_SYS_CTRL1	RW	System control high bit in USB host mode	0
4	bUC_SYS_CTRL0	RW	System control low bit in USB host mode	0
3	bUC_INT_BUSY	RW	Auto pause enable bit before the USB transfer completed interrupt flag is not cleared 1: Automatically pause before the UIF_TRANSFER interrupt flag is cleared. It will reply to the busy NAK in device mode. Automatically pause subsequent transfer in host mode . 0: Not pause.	0
2	bUC_RESET_SIE	RW	USB protocol processor software reset control bit. If this bit is 1, forced to reset the USB protocol processor and most of the USB control registers. It requires software to reset.	1
1	bUC_CLR_ALL	RW	If the bit is 1, empty USB interrupt flag and FIFO. It requires software to reset.	1
0	Reserved	RO	Reserved	0

When any one of bUC_HOST_MODE, bUC_SYS_CTRL1, bUC_DEV_SWAP, bUC_SYS_CTRL0 and bUC_DEV_EN is set to 1, P3.6/P3.7 GPIO function is disabled, and USB DP/DM function is enabled.

bUC_HOST_MODE, bUC_SYS_CTRL1 and bUC_SYS_CTRL0 control USB system together.

bUC_HOST_MODE	bUC_SYS_CTRL1 bUC_DEV_SWAP	bUC_SYS_CTRL0 bUC_DEV_EN	USB system control description
0	0	0	Disable USB device function. Disable DP/DM. Enable GPIO.

0	0	1	Enable USB device function. A 1.5KΩ pull-up resistor is required to be enabled. Configure bUDP_PUE, bUDM_PUE, bUD_LOW_SPEED and bUC_LOW_SPEED to 1000 when at full speed, and configure these bits to 0111 when at low speed. Disable other pull-up/pull-down resistors.
0	1	x	When bUD_LOW_SPEED=1 and bUC_LOW_SPEED=0, enable full-speed USB device function to swap DP/DM. It is required to set bUDM_PUE=1 to enable a 1.5KΩ pull-up resistor.
1	0	0	Select USB host mode. Normal working state.
1	0	1	Select USB host mode. Force DP/DM to output SE0 state.
1	1	0	Select USB host mode. Force DP/DM to output J state.
1	1	1	Select USB host mode. Force DP/DM to output K state / wakeup.

USB device address register (USB_DEV_AD):

Bit	Name	Access	Description	Reset value
7	bUDA_GP_BIT	RW	USB general purpose flag bit User-defined. Reset and set by software.	0
[6:0]	MASK_USB_ADDR	RW	Address of the USB device being operated in host mode. Address of the USB device in device mode.	00h

16.3 USB Device Register

In USB device mode, CH543 provides 4 sets of bidirectional endpoints (endpoint 0, endpoint 1, endpoint 2 and endpoint 3). The maximum data packet length of them is 64 bytes.

Endpoint 0 is the default endpoint and supports control transfer. The transmission and the reception share a 64-byte data buffer.

Endpoint 1, endpoint 2, endpoint 3 each includes a transmission endpoint (IN) and a reception endpoint (OUT). The transmission and the reception each has a separate 64-byte, supporting control transfer, bulk transfer, interrupt transfer, and simultaneous/synchronous transfer.

Each endpoint has a control register (UEPn_CTRL) and a transmission length register (UEPn_T_LEN, n=0/1/2/3), which are used to set the synchronization trigger bit of the endpoint, the response to OUT transactions and IN transactions, and the length of data to be sent.

As the necessary USB bus pull-up resistor of USB device, it can be set to be enabled or dosabled by software at any time. When bUDP_PUE or bUDM_PUE in USB_PULL is set to 1, CH543 internally connects a 1.5KΩ pull-up resistor with the DP pin or DM pin of the USB bus, and this is used for USB device function.

When a USB bus reset, or USB bus suspend/wakeup event is detected, or when the USB successfully processes data transmission/reception, the USB protocol processor sets the corresponding interrupt flag and generates an interrupt request. The application program can directly query, or it can query and analyze the interrupt flag register (USB_INT_FG) in the USB interrupt service program, and perform corresponding processing according to UIF_BUS_RST and UIF_SUSPEND. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze the USB interrupt status register (USB_INT_ST), and perform the corresponding processing according to the current endpoint number (MASK_UIS_ENDP) and the current transaction token PID (MASK_UIS_TOKEN). If the synchronization trigger bit (bUEP_R_TOG) of OUT transaction of each endpoint is set in advance, you can judge whether the synchronization trigger bit of the data packet received currently matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. Every time the USB transmit/receive interrupt is processed, the synchronization trigger bit of corresponding endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically toggle the corresponding synchronization trigger bit after successful transmission/reception.

The data to be sent by each endpoint is in their own buffer, and the length of the data to be sent is independently set in UEPn_T_LEN. The data received by each endpoint is in their own buffer, but the length of the data received is in the USB reception length register (USB_RX_LEN), and it can be distinguished according to the current endpoint serial number when the USB is receiving an interrupt.

Table 16.3.1 USB device registers (those marked in grey are controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
UDEV_CTRL	D1h	USB device physical port control register	0000 0000b
UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint 1 transmission length register	0000 0000b
UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
UEP2_T_LEN	D5h	Endpoint 2 transmission length register	0000 0000b
UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint 3 transmission length register	0000 0000b
UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint 0 transmission length register	0000 0000b
UEP0_DMA_L	ECh	Endpoint 0 buffer start address low byte	xxxx xxxxb
UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	xxxx xxxxb
UEP4_1_MOD	EAh	Endpoint 1, endpoint 4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint 2, endpoint 3 mode control register	0000 0000b

USB device physical port control register (UDEV_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
[7:3]	Reserved	RO	Reserved	00000b
2	bUD_LOW_SPEED	RW	USB device physical port low-speed mode enabled bit	0

			1: Low-speed mode (1.5Mbps) selected, or 12Mbps DP/DM swap mode selected. 0: Full-speed mode (12Mbps) selected.	
1	bUD_GP_BIT	RW	USB device mode general purpose flag bit User-defined. Reset and set by software.	0
0	bUD_PORT_EN	RW	USB device physical port enable bit 1: Physical port enabled. 0: Physical port disabled.	0

Endpoint n control register (UEPn_CTRL):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	Synchronization trigger bit expected by the receiver of USB endpoint n (handle SETUP/OUT transactions). 0: Expect DATA0. 1: Expect DATA1.	0
6	bUEP_T_TOG	RW	Synchronization trigger bit prepared by the transmitter of USB endpoint n (handle IN services). 0: Transmit DATA0. 1: Transmit DATA1.	0
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	Synchronization trigger bit auto toggle enable control bit 1: Auto toggle the corresponding synchronization trigger bit after sucessful transmission/reception. 0: No auto toggle, but manual switch is allowed. Only for endpoint 1/2/3.	0
3	bUEP_R_RES1	RW	Receiver of endpoint n to SETUP/OUT transactions response control high bit	0
2	bUEP_R_RES0	RW	Receiver of endpoint n to SETUP/OUT transactions response control low bit	0
1	bUEP_T_RES1	RW	Transmitter of endpoint n to IN transactions response control high bit	0
0	bUEP_T_RES0	RW	Transmitter of endpoint n to IN transactions response control low bit	0

MASK_UEP_R_RES, consisting of bUEP_R_RES1 and bUEP_R_RES0, is used to control the response of the receiver of endpoint n to the SETUP/OUT transactions. 00: represents reply ACK or ready. 01 represents timeout/no response, it is used for simultaneous/synchronous transfer of non-endpoint 0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

MASK_UEP_T_RES, consisting of bUEP_T_RES1 and bUEP_T_RES0, is used to control the response of the transmitter of endpoint n to the IN transactions. 00 represents reply DATA0/DATA1 or data ready or expected ACK. 01 represents reply DATA0/DATA1 and expected no response, which is used for simultaneous/synchronous transfer of non-endpoint 0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

Endpoint n transmission length register (UEPn_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes that USB endpoint n is ready to transmit	00h

USB endpoint 1, endpoint 4 mode control register (UEP4_1_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP1_RX_EN	RW	0: Endpoint 1 reception disabled. 1: Endpoint 1 reception enabled (OUT).	0
6	bUEP1_TX_EN	RW	0: Endpoint 1 transmission disabled. 1: Endpoint 1 transmission enabled (IN).	0
[5:0]	Reserved	RO	Reserved	00h

USB endpoint 2, endpoint 3 mode control register (UEP2_3_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP3_RX_EN	RW	0: Endpoint 3 reception disabled. 1: Endpoint 3 reception enabled (OUT).	0
6	bUEP3_TX_EN	RW	0: Endpoint 3 transmission disabled. 1: Endpoint 3 transmission enabled (IN).	0
[5:4]	Reserved	RO	Reserved	0
3	bUEP2_RX_EN	RO	0: Endpoint 2 reception disabled. 1: Endpoint 2 reception enabled (OUT).	0
2	bUEP2_TX_EN	RW	0: Endpoint 2 transmission disabled. 1: Endpoint 2 transmission enabled (IN).	0
[1:0]	Reserved	RO	Reserved	0

USB endpoint 0 receive/transmit share register (IN and OUT) takes UEP0_DMA as start address and the maximum packet length is 64 bytes.

USB endpoint 1/2/3 data buffer is selected by bUEPn_RX_EN and bUEPn_TX_EN(n=1/2/3). Refer to the following table.

Table 16.3.2 Endpoint n buffer modes (n=1/2/3)

bUEPn_RX_EN	bUEPn_TX_EN	Structure description: arrange from low to high with UEPn_DMA as the start address
0	0	Endpoint is disabled, and the UEPn_DMA buffer is not used.
1	0	Single 64-byte receive buffer (OUT)
0	1	Single 64-byte transmit buffer (IN)
1	1	Single 64-byte receive buffer. Single 64-byte transmit buffer.

USB endpoint n buffer start address (UEPn_DMA_L)(n=0/1/2/3):

Bit	Name	Access	Description	Reset value
[7:0]	UEPn_DMA_L	RW	Endpoint n buffer start address low byte. The high byte is always 0.	xxh

Note: The length of the receive buffer >= min (maximum data packet length possibly received + 2 bytes, 64 bytes).

16.4 Host Register

In USB host mode, CH543 provides 1 set of bidirectional host endpoint, including a transmission endpoint (OUT) and a reception endpoint (IN). The maximum data packet length is 64 bytes. The endpoint supports control transfer, bulk transfer, interrupt transfer, and simultaneous/synchronous transfer.

Each USB transaction initiated by host endpoint automatically sets the interrupt flag (UIF_TRANSFER) after processing. The application program can directly query, or it can query and analyze the interrupt flag register (USB_INT_FG) in the USB interrupt service program, and perform corresponding processing according to each interrupt flag. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze the USB interrupt status register (USB_INT_ST), and perform the corresponding processing according to the response PID (MASK_UIS_H_RES) of the current USB transfer transaction.

If the synchronization trigger bit (bUH_R_TOG) of IN transaction of host reception endpoint is set in advance, you can judge whether the synchronization trigger bit of the data packet received matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. Every time the USB transmit or receive interrupt is processed, the synchronization trigger bit of corresponding host endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically toggle the corresponding synchronization trigger bit after successful transmission/reception.

USB host token setting register (UH_EP_PID) is a multiplexing of the USB endpoint 2 control register in USB device mode, which is used to set the endpoint number of the target device being operated and the token PID of the USB transfer transaction. The data corresponding to the SETUP token and OUT token is provided by the host transmission endpoint. The data to be sent is in the UH_TX_DMA buffer, and the length of the data to be sent is set in UH_TX_LEN. The data corresponding to the IN token is returned by the target device to the host reception endpoint, the received data is stored in the UH_RX_DMA buffer, and the received data length is stored in USB_RX_LEN.

Table 16.4.1 USB host registers (those marked in grey are controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
UHOST_CTRL	D1h	USB host physical port control register	0000 0000b
UH_SETUP	D2h	USB host auxiliary setting register	0000 0000b
UH_RX_CTRL	D4h	USB host reception endpoint control register	0000 0000b
UH_EP_PID	D5h	USB host token setting register	0000 0000b
UH_TX_CTRL	D6h	USB host transmission endpoint control register	0000 0000b
UH_TX_LEN	D7h	USB host transmission length register	0000 0000b
UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb
UH_EP_MOD	EBh	USB host endpoint mode control register	0000 0000b

USB host physical port control register (UHOST_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
[7:3]	Reserved	RO	Reserved	00000b
2	bUH_LOW_SPEED	RW	USB host port low-speed mode enable bit 1: Low speed mode, 1.5Mbps. 0: Full speed mode, 12Mbps.	0
1	bUH_BUS_RESET	RW	USB host port bus reset control bit 1: Force the host port to output USB bus reset. 0: End the output.	0
0	bUH_PORT_EN	RW	USB host port enable bit 0: Host port disabled. 1: Host port enabled. The bit is cleared automatically when the USB device is disconnected.	0

USB host auxiliary setting register (UH_SETUP):

Bit	Name	Access	Description	Reset value
7	bUH_PRE_PID_EN	RW	Low speed preamble packet PRE PID enable bit 1: USB host enabled to communicate with the low-speed USB device via external HUB. 0: Low speed preamble packet disabled, and there should be no HUB between the USB host and low-speed USB device.	0
6	bUH_SOF_EN	RW	SOF packet auto generate enable bit 1: USB host automatically generates the SOF packet. 0: SOF packet is not generated automatically, but can be generated manually.	0
[5:0]	Reserved	RO	Reserved	00h

USB host reception endpoint control register (UH_RX_CTRL):

Bit	Name	Access	Description	Reset value
7	bUH_R_TOG	RW	Synchronization trigger bit expected by the receiver of USB host (handle IN services). 0: Expect DATA0. 1: Expect DATA1.	0
[6:5]	Reserved	RO	Reserved	00b
4	bUH_R_AUTO_TOG	RW	Auto toggle bUH_R_TOG enable control bit 1: Auto toggle the bUH_R_TOG flag after successfully received by the USB host. 0: No auto toggle, but manual switch is allowed.	0

3	Reserved	RO	Reserved	0
2	bUH_R_RES	RW	Response control bit of USB host receiver for IN transaction 0: Reply ACK or ready. 1: No reponse, which is used for simultaneous/synchronous transfer with non-endpoint 0 of the target device	0
[1:0]	Reserved	RO	Reserved	00b

USB host token setting register (UH_EP_PID):

Bit	Name	Access	Description	Reset value
[7:4]	MASK_UH_TOKEN	RW	Set the token PID of this USB transfer transaction	0000b
[3:0]	MASK_UH_ENDP	RW	Set the endpoint serial number of the target device being operated this time	0000b

USB host transmission endpoint control register (UH_TX_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_T_TOG	RW	Synchronization trigger bit prepared by the transmitter of USB host (handle SETUP/OUT transactions). 0: Transmit DATA0. 1: Transmit DATA1	0
5	Reserved	RO	Reserved	0
4	bUH_T_AUTO_TOG	RW	Auto toggle bUH_T_TOG enable control bit 1: Auto toggle the bUH_T_TOG flag after successfully transmitted by the USB host. 0: No auto toggle, but manual switch is allowed.	0
[3:1]	Reserved	RO	Reserved	000b
0	bUH_T_RES	RW	Response control bit of USB host transmitter for SETUP/OUT transaction 0: Expect reply ACK or ready. 1: Expect no reponse, which is used for simultaneous/synchronous transfer with non-endpoint 0 of the target device.	0

USB host transmission length register (UH_TX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_LEN	RW	Set the number of data bytes that USB host transmission	00h

			endpoint is ready to send	

USB host endpoint mode control register (UH_EP_MOD):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_EP_TX_EN	RW	0: USB host transmission endpoint disabled to transmit data. 1: USB host transmission endpoint enabled to transmit data (SETUP/OUT), with UH_TX_DMA as start address. Single 64-byte transmit buffer.	0
[5:4]	Reserved	RO	Reserved	00b
3	bUH_EP_RX_EN	RO	0: USB host reception endpoint disabled to receive data. 1: USB host reception endpoint enabled to receive data (IN), with UH_RX_DMA as start address. Single 64-byte receive buffer.	0
[2:0]	Reserved	RO	Reserved	000b

USB host receive buffer start address(UH_RX_DMA_L):

Bit	Name	Access	Description	Reset value
[7:0]	UH_RX_DMA_L	RW	Host receive buffer start address low byte. The high byte is always 0.	xxh

USB host transmit buffer start address (UH_TX_DMA_L):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_DMA_L	RW	Host transmit buffer start address low byte. The high byte is always 0.	xxh

17. Inter-integrated Circuit (I2C) Interface

17.1 I2C Introduction

CH543 and CH541 provide I2C slave (I2CS) interface.

Main features:

(1). I2C slave controller, supports several interrupts, and supports 100KHz, 400KHz and 1MHz and other transfer rates.

(2). Presettable slave address. Support broadcast address.

(3). For low-speed applications, the pull-up resistor on I2C pin can be used directly.

17.2 I2C Register

Table 17.2.1 I2C registers

Name	Address	Description	Reset value
I2CS_CTRL	A4h	I2CS slave control register	0000 0x00b
I2CS_DEV_A	A5h	I2CS slave device address register	0000 0000b
I2CS_ADDR	A6h	I2CS slave data address register (read only)	xxxx xxxxb
I2CS_DATA	A7h	I2CS slave data receive/transmit register	xxxx xxxxb
I2CS_STAT	A0h	I2CS slave status register	0000 1100b

I2CS slave control register (I2CS_CTRL):

Bit	Name	Access	Description	Reset value
7	bI2CS_IE_READ	RW	I2CS read data interrupt enable bit 1: Interrupt triggered after a byte is transmitted. 0: Interrupt not triggered.	0
6	bI2CS_IE_WRITE	RW	I2CS written data interrupt enable bit 1: Interrupt triggered after a byte is received. 0: Interrupt not triggered.	0
5	bI2CS_IE_ADDR	RW	I2CS receive data address interrupt enable bit 1: Interrupt triggered after the data address is received. 0: Interrupt not triggered.	0
4	bI2CS_IE_DEV_A	RW	I2CS receive slave address interrupt enable bit 1: Interrupt triggered after the slave address is received. 0: Interrupt not triggered. If this bit is 1, the broadcast address is enabled. Otherwise it is not supported.	0
3	bI2CS_IE_STASTO	RW	I2CS receive START or STOP condition interrupt enable bit 1: Interrupt triggered after START/STOP is received. 0: Interrupt not triggered.	0
2	bI2CS_SDA_IN	RO	Current state of SDA pin after synchronization: 0: Low level. 1: High level.	x

1	Reserved	RO	Reserved	0
0	bI2CS_EN	RW	I2CS slave enable 0: I2CS slave disabled and cleared. 1: I2CS slave enabled.	0

I2CS slave device address register (I2CS_DEV_A):

Bit	Name	Access	Description	Reset value
[7:1]	MASK_I2CS_DEV_A	RW	I2CS slave device address 0: Broadcast address. Others: Assigned slave device address that needs to be matched.	00h
[3:1]	bI2CS_DEV_A3H	RO	Store the higher 3 bits of the data unit address specified by the external I2C master, available only when bI2CS_DA_4BIT=1	xxxb
0	bI2CS_DA_4BIT	RW	I2CS slave device address mode: 0: 7-bit slave address mode. I2CS_ADDR is actually 8-bit. 1: 4-bit slave address mode. Only the higher 4 bits of slave device address need to be matched, and the lower 3 bits do not need to be matched. The lower 3 bits of the slave device address being operated are stored in bI2CS_DEV_A3H. I2CS_ADDR actually is extended to 11 bits. The higher 3 bits are from bI2CS_DEV_A3H.	0

I2CS slave data address register (I2CS_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_ADDR	RO	Store the data unit address specified by the external I2C host, which is automatically increased after each byte during a sequential read-write operation.	xxh

I2CS slave data receive/transmit register (I2CS_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_DATA	RW	I2CS slave data receive/transmit register includes a transmit register and a receive register that are physically separated. The data written into this register is used to be transmitted and for external I2C master to read. Reading this register returns the data in the receive buffer, and the data is usually the data written by the external I2C master recently.	xxh

I2CS slave status register(I2CS_STAT):

Bit	Name	Access	Description	Reset value
7	I2CS_IF_STASTO	RW	Receive START or STOP condition interrupt flag bit 1: There is an interrupt. Judge whether it is START or STOP according to MASK_I2CS_STAT. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
6	I2CS_IF_BYTE	RW	A byte transmit completed interrupt flag bit 1: Interrupt, triggered at the end of a byte reception or transmission. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
5	I2CS_IF_ADDR	RW	Receive data unit address interrupt flag bit 1: Interrupt, triggered after the data address is received. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	I2CS_IF_DEV_A	RW	Receive slave device address interrupt flag bit 1: Interrupt, triggered after the slave address is received, no matter whether the address is matched. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
[3:0]	MASK_I2CS_STAT	RO	Current state of I2CS slave: 0000: Free, or it is receiving the slave address. 0001: Respond to the received slave address. 0010: It is receiving the data unit address. 0011: Respond to the received data unit address. 0100: It is receiving the data byte. 0101: Respond to the received data byte. 0110: It is transmitting data byte. 0111: It is waiting and checking the response after data transmission. 1100: In STOP condition. XXXX: Unknown state.	1100b

18. USB PD and Type C Controller

18.1 PD and Type C Introduction

CH541 supports USB type-C only. CH543 supports USB type-C, USB PD and PD 3.0. CH543 also supports programmable supply currents for PMU regulation of external supply voltages and supports PD 3.0 and PPS.

Main features:

(1): Built-in USB type-C interface, supports master/slave detection, supports DRP, Sink/Consumer and Source/Provider.

(2). Built–in USB PD transceiver PHY. Integrated hardware edge slope control.

(3). Built–in USB Power Delivery controllet, automatic BMC encoder/decoder, 4b5b encoder/decoder and CRC.

(4). Supports SOP, SOP', SOP" and other PD packets. Support hardware reset the USB PD reset signal frame.

(5): Up to 123-byte data packet. DMA capability.

(6). Supports USB PD 2.0 and 3.0 power delivery protocols. USB port supports BC and other charging protocols.

18.2 PD and Type C Register

Table 18.1.1 PD and type C registers

Name	Address	Description	Reset value
CC1_CTRL	C6h	PD/type C CC1 control register	0000 0011b
CC2_CTRL	C7h	PD/type C CC2 control register	0000 0011b
UPD_INT_FG	C0h	PD interrupt flag register	0000 0000b
UPD_INT_EN	C1h	PD interrupt enable register	0000 0000b
UPD_CTRL	C2h	PD control register	0000 0010b
UPD_DATA	C3h	PD data register	xxxx xxxxb
UPD_DMA_L	C4h	PD buffer start address low byte	xxxx xxxxb
UPD_TIMER	BBh	PD BMC timer register	0000 0000b
UPD_COUNT	BCh	PD data byte count register (read only)	0xxx xxxxb
UPD_T_LEN	BDh	PD transmission length register	0000 0000b
UPD_T_SOP	BEh	PD transmit SOP configuration register	0000 0000b
UPD_CRC32	BFh	PD CRC32 data check register (read only)	xxxx xxxxb

PD/type C CC1 and CC2 control registers (independently controlled by CC1_CTRL and CC2_CTRL):

Bit	Name	Access	Description	Reset value
7	bCC_CE	RW	CC1/CC2 port voltage comparator enable: 0: Comparator disabled. By default, bCC_CMPO outputs 1. 1: : Comparator enabled. Reference voltage is selected by MASK_CC_CVS.	0
6	bCC_LVO	RW	CC1/CC2 port low voltage output mode enable: 0: Normal voltage (VDD) drive output.	0

			1: PD low voltage drive output.	
5	bCC_CVS1	RW	Reference voltage of port voltage comparator selected by MASK_CC_CVS: 00: 0.55V. 01: 0.22V. 10: 0.66V. 11: 1.23V.	0
4	bCC_CVS0	RW		0
3	bCC_PU1	RW	CC1/CC2 port pull-up current selected by MASK_CC_PU: 00: Pull-up current disabled. 01: About 330uA pull-up current. 10: About 180uA pull-up current. 11: About 80uA pull-up current.	0
2	bCC_PU0	RW		0
1	bCC_PD	RW	CC1/CC2 port pull-down resistor enable: 0: Pull-down resistor disabled. 1: 5.1KΩ pull-down resistor enabled.	1
0	bCC_CMPO	RO	CC1/CC2 port voltage comparator result output bit: 0: Current port voltage is less than the reference voltage. 1: Current port voltage is more than the reference voltage.	1

USB PD interrupt flag register (UPD_INT_FG):

Bit	Name	Access	Description	Reset value
7	PIF_TX_END	RW	PD transmit data packet completed interrupt flag bit 1: Interrupt, triggered by the completion of the data packet transmission. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
6	PIF_RX_RST	RW	PD receive reset signal frame interrupt flag bit 1: Interrupt, triggered by the completion of the reset signal frame reception, specifically distinguished by MASK_PD_STAT. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
5	PIF_RX_ACT	RW	PD receive data packet interrupt flag bit 1: Interrupt, triggered by the completion of data packet reception, specifically distinguished by MASK_PD_STAT. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	PIF_RX_BYTE	RW	PD receive data byte interrupt flag bit 1: Interrupt, triggered by the completion of SOP reception or by the completion of data byte reception, specifically distinguished by MASK_PD_STAT and UPD_COUNT. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit	0

			in the register to reset.	
3	PIF_RX_BIT	RW	PD receive data bit interrupt flag bit 1: Interrupt, triggered by the completion of one symbol, ie 5bit reception (if bPIE_RX_BYTE=1) or by the completion of one bit reception (if bPIE_RX_BYTE=0). 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
2	PD_START	RW	PD transmit control bit when bPD_TX_EN=1. Set to 1 to start PD transmission. PHY automatically switches to output. This bit is cleared automatically at the end of transmission. PD receive enable bit when bPD_TX_EN=0 and bCC_CE selected by bPD_CC_SEL is 1. Set to 1 to enable PD reception. Set to 0 to disabled PD reception.	0
1	PD_STAT1	RO	MASK_PD_STAT indicate current PD state, provide specific details. When PD is receiving, or after PD reception is completed, state is as follows: 00: Free, or receive no valid data packet. 01: Receive SOP, ie SOP0. 10: Receive SOP' , ie SOP1 or Hard Reset. 11: Receive SOP", ie SOP2 or Cable Reset. During PD transmission, state is as follows: 00: CRC32[7:0] are being transmitted. 01: CRC32[15:8] are being transmitted. 10: CRC32[23:16] are being transmitted. 11: CRC32[31:24] are being transmitted.	0
0	PD_STAT0	RO		0

PD interrupr enable register (UPD_INT_EN):

Bit	Name	Access	Description	Reset value
7	bPIE_TX_END	RW	1: PD transmit data packet completed interrupt enabled. 0: PD transmit data packet completed interrupt disabled.	0
6	bPIE_RX_RST	RW	1: PD receive reset signal frame interrupt enabled. 0: PD receive reset signal frame interrupt disabled.	0
5	bPIE_RX_ACT	RW	1: PD receive data packet interrupt enabled. 0: PD receive data packet interrupt disabled.	0
4	bPIE_RX_BYTE	RW	1: PD receive data byte interrupt enabled. 0: PD receive data byte interrupt disabled.	0
3	bPIE_RX_BIT	RW	1: PD receive data bit interrupt enabled. 0: PD receive data bit interrupt disabled.	0
2	bPIE_CC_IO	RW	CC port voltage comparator result change interrupt enable if bCC_CE of CC1 or CC2 selected by bPD_CC_SEL is 1: 1: CC port voltage comparator result change interrupt enabled.	0

			0: CC port voltage comparator result change interrupt disabled. Clearing bPIE_CC_IO causes that internal interrupt flag is cleared at the same time. GPIO level change interrupt enable when bCC_CE selected by bPD_CC_SEL is 0: 1: P1.0/P1.1 level change interrupt enabled. 0: Interrupt disabled. Usually, PD must be set to 0 during reception.	
1	bPD_CRC32_SEL1	RW	MASK_PD_CRC_SEL selects CRC32 data bit presented by UPD_CRC32: 00: [7:0] data bits for reading. 01: [15:8] data bits for reading. 10: [23:16] data bits for reading. 11: [31:24] data bits for reading. This bit is cleared automatically when bPD_CLR_ALL=1, or when reading/writing to UPD_INT_EN. Automatically adds 1 after UPD_CRC32 is read. Loopback is supported.	0
0	bPD_CRC32_SEL0	RW		0

P1.0/P1.1 level change interrupt:

When bCC_CE selected by bPD_CC_SEL is 0 and bPIE_CC_IO=1, GPIO level change interrupt is automatically enabled for P1.0 or P1.1 in high-impendance input mode. If P1_MOD_OC[0]=0 and P1_DIR_PU[0]=0, PD interrupt is generated when P1.0 input state is different from the value in P1.0 output register. The interrupt request is cancelled after updating the value in the output register with the new state of P1.0 pin. P1.1 is similar to it. In addition, both P1.0 and P1.1 level change interrupts can be enabled.

PD control register (UPD_CTRL):

Bit	Name	Access	Description	Reset value
7	bPD_NIBBLE_HI	RO	Current half-byte state during PD receprion/transmission 0: The lower 4 bits are being processed. 1: The higher 4 bits are being processed.	0
6	bBMC_TX_BIT_B	RO	Current bit state when BMC transmits encoding 0: The first half is being processed. 1: The second half is being processed.	0
5	bPD_WAKE_POLAR	RW	Polarity of comparison result or I/O for PD wakeup 0: Low for effective wakeup. 1: High for effective wakeup.	0
4	bPD_RST_EN	RW	Execution function after PD reset signal frame is received: 0: PIF_RX_RST enabled after PD reset signal frame is received. If bPIE_RX_RST=1, PD interrupt is generated. 1: Reset the chip after Hard Reset is received. If bPIE_RX_RST=1, receiving Cable Reset also causes chip reset.	0
3	bPD_DMA_EN	RW	1: PD DMA enabled.	0

			0: PD DMA disabled.	
2	bPD_CC_SEL	RW	PD receive/transmit port selection: 0: P1.0/CC1 selected. 1: P1.1/CC2 selected.	0
1	bPD_CLR_ALL	RW	1: Clear PD interrupt flag and FIFO. It requires software to reset. 0: PD IO function enabled.	1
0	bPD_TX_EN	RW	PD transmit enable: 0: PD transmit disabled. If bCC_CE selected by bPD_CC_SEL is 1, this CC channel is enabled to receive. 1: Transmission enabled on the CC channel selected by bPD_CC_SEL.	0

USB PD system is controlled by bPD_CLR_ALL, bCC_CE selected by bPD_CC_SEL, and bPD_TX_EN:

bPD_CLR_ALL	Selected bCC_CE	bPD_TX_EN	USB PD system control description
1	0	0	Disabled PD function. P1.0/P1.1 as GPIO.
0	0	0	Enable PD clock and I/O. Disable GPIO.
0	1	0	Enable CC port voltage comparator. Then PD receive enabled by PD_START.
0	x	1	PD transmit enable. After bCC_LVO is set to 1, PD transmit enabled by PD_START.

PD wakeup signal source and polarity:
When bPD_CC_SEL=0, P1.0/CC1 signal and P1.1/CC2 signal are supported to wake up PD. When bPD_CC_SEL=1, only P1.1/CC2 signal is supported to wake up PD.

Either analog comparison result or pin digital level is selected by bCC_CE. When bCC_CE of CC1 is 1, CC1 port voltage comparator result is selected to wake up PD. When bCC_CE of CC1 is 0, CC1 level is s selected to wake up PD.

bPD_WAKE_POLAR selects the signal polarity. When bPD_WAKE_POLAR=0, the comparator result low or pin low level is selected to wake up PD. When bPD_WAKE_POLAR=1, the comparator result high or pin high level is selected to wake up PD.

CC2 is similar to CC1. Selected by bCC_CE of CC2.

PD data register (UPD_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	UPD_DATA	RW	1-byte buffer for PD reception/transmission. If DMA is not enabled, query bPD_NIBBLE_HI to write data to this register for transmission when transmitting. Read this register after PIF_RX_BYTE interrupt to return the received data byte when receiving.	xxh

PD buffer start address (UPD_DMA_L):

Bit	Name	Access	Description	Reset value
[7:0]	UPD_DMA_L	RW	PD buffer start address low byte. The high byte is always 0. Count of bytes that actually occupy the buffer is UPD_COUNT.	xxh

PD BMC timing register (UPD_TIMER):

Bit	Name	Access	Description	Reset value
[7:0]	UPD_TIMER	RW	Adjust the timing value of PD BMC encoder/decoder. To apply to different system clock frequencies (Fsys), or to adjust PD communication rate, the encoding timing value needs to be written before PD transmits, and the decoding timing value needs to be written before PD receives.	00h

PD data byte count register (UPD_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	UPD_COUNT	RO	Current count of data bytes transferred by PD packet. For transmission, these bits indicate the current count of data bytes after entering the dat phase. For reception, these bits indicate the current count of the received data bytes. Subtract 4 from this value to get the number of bytes in the packet without 32-bit CRC.	00h

PD transmission length register (UPD_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	UPD_T_LEN	RW	The number of dat bytes transmitted by PD, without CRC. After the data packet transmission is completed, 32-bit CRC and EOP terminator are automatically added and then transmitted.	00h

PD transmit SOP configuration register (UPD_T_SOP):

Bit	Name	Access	Description	Reset value
[7:6]	bUPD_KC4	RW	The PD transmit SOP configuration is formed by combining 4 symbols. Provides predefined: UPD_SOP0/SOP, UPD_SOP1/SOP', UPD_SOP2/SOP", UPD_HARD_RESET, UPD_CABLE_RESET	00b
[5:4]	bUPD_KC3	RW		00b
[3:2]	bUPD_KC2	RW		00b
1	Reserved	RO		0
0	bUPD_KC1	RW		0

PD CRC32 data check register (UPD_CRC32):

Bit	Name	Access	Description	Reset value
[7:0]	UPD_CRC32	RO	CRC32 data check window. Data bit required to be checked is selected by MASK_PD_CRC_SEL.	xxh

18.3 PD Application

18.3.1 PD Reception Configuration and Application

(1). Initiate type C port. Set I/O pin used for CC to high-impendance input. Set bCC_CE=1, MASK_CC_CVS=00, and bCC_LVO=0 for the selected CC port. In addition, keep or change MASK_CC_PU or bCC_PD according to the actual situation.

(2). Set bPD_CLR_ALL=0. Select bPD_CC_SEL. Set bPD_TX_EN=0 for reception. Set bPD_DMA_EN and bPD_RST_EN as required.

(3). Optional, set UPD_INT_EN and IE_USBPD. Usually, set bPIE_RX_ACT=1, and set bPIE_RX_RST as required.

(4). If DMAis enabled, it is required to set UPD_DMA_L in advance.

(5). According to the system clock frequency, load the corresponding decoding timing value (UPD_TMR_RX_*) for UPD_TIMER.

(6). Set PD_START=1 to enable reception.

(7). After the receive completed interrupt, or after the reception completion is queried, analyze MASK_PD_STAT and process the data packet. UPD_COUNT minus 4 is the data length, and it can automatically continue to receive the next packet. If there is no subsequent reception, PD_START can be disabled.

18.3.2 PD Transmission Configuration and Application

(1). Initiate type C port. Set I/O pin used for CC to high-impendance input. Set bCC_LVO=0 for the selected CC port. bCC_CE and MASK_CC_CVS do not affect it. In addition, keep or change MASK_CC_PU or bCC_PD according to the actual situation.

(2). Set bPD_CLR_ALL=0. Select bPD_CC_SEL. Set bPD_TX_EN=1 for transmission. Set bPD_DMA_EN as required.

(3). Optional, set UPD_INT_EN and IE_USBPD. Usually, set bPIE_TX_END=1.

(4). If DMAis enabled, it is required to set UPD_DMA_L in advance.

(5). According to the system clock frequency, load the corresponding encoding timing value (UPD_TMR_TX_*) for UPD_TIMER.

(6). Prepare data. Set UPD_T_SOP and UPD_T_LEN.

(7). Set bCC_LVO=1 for the selected CC port. Set PD_START=1 to startup transmission immediately. It is cleared automatically at the end of transmission.

(8). After the transmit completed interrupt, or after the transmission completion is queried, set bCC_LVO=0 at once for the selected CC port.

(9). You can set bCC_LVO=1 and PD_START=1 again to start to transmit next packet.

18.3.3 Recommended Configuration and Application for PD Receive and Transmit Switch

(1). Initiate type C port. Set the used I/O pin to high-impendance input (corresponding bit os P1_DIR_PU/P1_MOD_OC is 0). Set bCC_CE=1, MASK_CC_CVS=00 and bCC_LVO=0 for the selected CC port, for both reception and transmission. Reduce frequent changes during receive/transmit switch. In addition. MASK_CC_PU or bCC_PD maintains the actual settings of the

previous type C master/slave negotiation.

(2). Set bPD_CLR_ALL=0. Select bPD_CC_SEL. Set bPD_TX_EN=0 for reception by default. It is recommended to set bPD_DMA_EN.

(3). Clear interrupt flags. It is recommended to set UPD_INT_EN and IE_USBPD, set bPIE_RX_ACT=1, and set bPIE_TX_END=1.

(4). For applications where the transmit SOP configuration is basically unchanged, preset UPD_T_SOP here.

(5). According to the position of the receive/transmit buffer, set UPD_DMA_L in advance. If the receive buffer and the transmit buffer share a buffer, there is no need to change it later.

(6). According to the system clock frequency, load the corresponding decoding timing value (UPD_TMR_RX_*) for UPD_TIMER.

(7). Set PD_START=1 to enable reception.

(8). After the receive completed interrupt, disable PD_START to pause reception. Analyze MASK_PD_STAT and process data packet.

(9). Enter half-duplex transmission state. Prepare the data to be transmitted in the buffer.

(10). According to the system clock frequency, load the corresponding encoding timing value (UPD_TMR_TX_*) for UPD_TIMER.

(11). Set UPD_T_LEN. If the receive buffer and the transmit buffer are separate, switch UPD_DMA_L here. If it is required to be changed to transmit SOP, update UPD_T_SOP here. Delay the interval to wait for the PD protocol as needed.

(12). Set bPD_TX_EN=1 to switch to transmit mode.

(13). Set bCC_LVO=1 for the selected CC port. Set PD_START=1 immediately to startup transmission. It is cleared automatically at the end of transmission.

(14). After the transmit completed interrupt, set bCC_LVO=0 for the selected CC port at once. You can set bPD_TX_EN=0 to switch to default receive mode.

(15). Turn to step (5) to prepare the reception of next packet.

19. Parameters

19.1 Absolute Maximum Ratings

Operating in critical ratings or exceeding the absolute maximum ratings may cause the chip to work abnormally or even be damaged.

Symbol	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	Rated 5V or 9V, VDD12<10V, Fsys<40MHz	-40	85	℃
		Rated 12V, VDD12>=10V, Fsys<40MHz	-20	70	℃
TAROM	Ambient temperature when performing erase/write operation on Flash-ROM/EEPROM (recommended)		-20	85	℃
TS	Storage ambient temperature		-55	125	℃
VDD12	Supply voltage (VDD12 is connected to power, GND to ground)		-0.4	13.5	V
VDD	Internal USB and I/O supply voltage		-0.4	6.0 VDD12+0.4	V
VIO	Voltage on input/output pins except P3.5 or RST		-0.4	VDD+0.4	V
VIOHV	Voltage on P3.5 and RST		-0.4	VDD12+0.4	V
TVRISE	VDD12 voltage rise time (avoid instantaneous high voltage power-on within nanoseconds)		1	500000	uS/V

19.2 Electrical Characteristics (3.3V)

Test conditions: TA=25℃, VDD12=5V&VDD=3.3V or VDD12=VDD=3.3V, Fsys=12MHz.

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD12	VDD12 pin supply voltage	VDD is only connected to an external capacitor	3.7	5	12.6	V
		VDD is shorted to VDD12	2.8	3.3	3.6	V
VDD	Internal power regulator output voltage (Automatically shorted to VDD12 during sleep)	TA=-15～65℃	3.23	3.3	3.45	V
		TA=-40～85℃	3.2	3.3	3.5	V
VDD	VDD pin supply voltage	VDD is shorted to VDD12, with USB ON	3.0	3.3	3.6	V
		VDD is shorted to VDD12, with USB OFF	2.8	3.3	3.6	V
ICC24M3	Total supply current when Fsys=24MHz			4.3		mA
ICC12M3	Total supply current when Fsys=12MHz			2.9		mA
ICC750K3	Total supply current when Fsys=750KHz			1.4		mA
ISLP3	Total supply current in Halt mode			0.3	0.6	mA
ISLP3L	Total supply current after power-down/deep-sleep, with bLDO_3V3_OFF=1, LDO disabled			4	20	uA
IADC3	ADC operating current			180	500	uA

ICMP3	Voltage comparatoe module operating current		80	240	uA
ITKEY3	Capacitive touch-key charging current	30	50	70	uA
VIL3	Input low level voltage	0		0.8	V
VIH3	Input high level voltage	2.0		VDD	V
VIHP4	P1.0/1.1/P3.6/3.7 input high level voltage	2.2		VDD	V
VIH3H	P3.5/RST input high level voltage	2.0		VDD12	V
VOL3	Output low level voltage (12mA sunk current)			0.4	V
VOH3	Output high level voltage (6mA sourced current)	VDD-0.4			V
VOH3PD	P1.0/1.1 output high level voltage (1mA sourced current)	VDD-0.6			V
VOL3U	P3.5/6/7 output low level voltage (8mA sunk current)			0.4	V
VOH3U	P3.6/3.7 output high level voltage (8mA sourced current)	VDD-0.4			V
VOH35	P3.5 output high level voltage (2mA sourced current)	VDD12-0.4			V
VADCPD	AIN0/1/3 ADC active input high voltage range	VDD-0.8	VDD-0.5		V
ICMP	CMP output drive capability	120	180		uA
IIN	Sunk current of input without pull-up resistor	-5	0	5	uA
IUP3	Sunk current of non-dedicated input with pull-up resistor	15	30	50	uA
IUP3X	Sunk current of input with pull-up resistor from low to high	100	170	260	uA
ISSTEP	ISINK programmable step (average value) of irrigation current		0.465		uA
V3REF	Relative error of ADC internal channel VREF12 reference voltage	-7%	±2%	+7%	
ISDIF	Error of ISINK programmable sink current (at full amplitude)	-3.5%	±1%	+3.5%	
I3DIF	USB and USB PD pull-up/pull-down current error	-30%	±7%	+20%	
R3DIF	USB and USB PD pull-up/pull-down resistor error	-20%	±7%	+20%	
RU1K5	1.5KΩ pull-up resistor on USB pin	1.3	1.5	1.75	KΩ
RR40K	40KΩ pull-down resistor on RST pin	35	40	46	KΩ
Rsw3	Analog switch ON resistor of ADC and other modules	500	700	2000	Ω
Vovr	VDD12 over-voltage reset threshold	13.0	14.5	17.5	V
Vpot	Power on reset threshold	2.2	2.3/2.8	3.0	V

19.3 Electrical Characteristics (4.7V)

Test conditions: TA=25°C, VDD12=5.5V&VDD=4.7V or VDD12=VDD=4.7V, Fsys=12MHz.

Symbol	Parameter description	Min.	Typ.	Max.	Unit

VDD12	VDD12 pin supply voltage	VDD is only connected to an external capacitor	5.2	5.5	12.6	V
VDD	Internal power regulator output voltage (Automatically shorted to VDD12 during sleep)	TA=-15～65℃	4.6	4.7	4.85	V
		TA=-40～85℃	4.56	4.7	4.9	V
VDD	VDD pin supply voltage (VDD is shorted to VDD12)		4.0	4.7	5.5	V
ICC24M5	Total supply current when Fsys=24MHz			4.4		mA
ICC12M5	Total supply current when Fsys=12MHz			3.0		mA
ICC750K5	Total supply current when Fsys=750KHz			1.5		mA
ISLP5	Total supply current in Halt mode			0.3	0.7	mA
ISLP5L	Total supply current after power-down/deep-sleep, with bLDO_3V3_OFF=1, LDO disabled			6	30	uA
IADC5	ADC operating current			200	600	uA
ICMP5	Voltage comparatoe module operating current			100	300	uA
ITKEY5	Capacitive touch-key charging current		30	50	70	uA
VIL5	Input low level voltage		0		1.2	V
VIH5	Input high level voltage		2.6		VDD	V
VIHP6	P1.0/1.1/P3.6/3.7 input high level voltage		3.0		VDD	V
VIH5H	P3.5/RST input high level voltage		2.6		VDD12	V
VOL5	Output low level voltage (20mA sunk current)				0.4	V
VOH5	Output low level voltage (10mA sourced current)		VDD-0.4			V
VOH5PD	P1.0/1.1 output high level voltage (1mA sourced current)		VDD-0.6			V
VOL5U	P3.5/6/7 output low level voltage (10mA sunk current)				0.4	V
VOH5U	P3.6/3.7 output high level voltage (10mA sourced current)		VDD-0.4			V
VOH35	P3.5 output high level voltage (4mA sourced current)		VDD12-0.4			V
VADCPD	AIN0/1/3 ADC active input high voltage range		VDD-0.9	VDD-0.6		V
ICMP	CMP output drive capability		160	240		uA
IIN	Sunk current of input without pull-up resistor		-5	0	5	uA
IUP5	Sunk current of non-dedicated input with pull-up resistor		35	70	110	uA
IUP5X	Sunk current of input with pull-up resistor from low to high		250	400	600	uA
ISSTEP	ISINK programmable step (average value) of irrigation current			0.465		uA
V5REF	Relative error of ADC internal channel VREF12 reference voltage		-8%	±2%	+8%	

ISDIF	Error of ISINK programmable sink current (at full amplitude)	-4%	±1%	+4%	
I5DIF	USB and USB PD pull-up/pull-down current error	-30%	±8%	+24%	
R5DIF	USB and USB PD pull-up/pull-down resistor error	-24%	±8%	+24%	
RU1K5	1.5KΩ pull-up resistor on USB pin	1.2	1.5	1.7	KΩ
RR40K	40KΩ pull-down resistor on RST pin	35	40	46	KΩ
Rsw5	Analog switch ON resistor of ADC and other modules	300	450	1000	Ω
Vovr	VDD12 over-voltage reset threshold	13.0	14.5	17.5	V
Vpot	Power on reset threshold	2.2	2.3/2.8	3.0	V

19.4 Timing Parameters

Test conditions: TA=25°C, VDD12=5V&VDD=3.3V or VDD12=VDD=3.3V, Fsys=12MHz.

Symbol	Parameter description		Min.	Typ.	Max.	Unit
Fosc	Internal clock frequency after calibration when VDD12>=3V	TA=-15～65°C	47.1	48	48.9	MHz
		TA=-40～85°C	46.8	48	49.2	MHz
Fosc3	Internal clock frequency after calibration when VDD12<3V		46.5	48	49.5	MHz
Tpor	Power on reset delay		8	11	15	mS
Trst	External input valid reset signal width from RST		2			uS
Trdl	Thermal reset delay		20	30	50	uS
Twdc	Watchdog overflow cycle/ timing cycle calculation formula		131072 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	USB auto suspended time in USB host mode		2	3	4	mS
	USB auto suspended time in USB device mode		4	5	6	mS
Twakht	Time to wake up from halt mode		0.5	1	3	uS
Twakdp	Time to wake up from power-down/deep-sleep		120	200	1000	uS

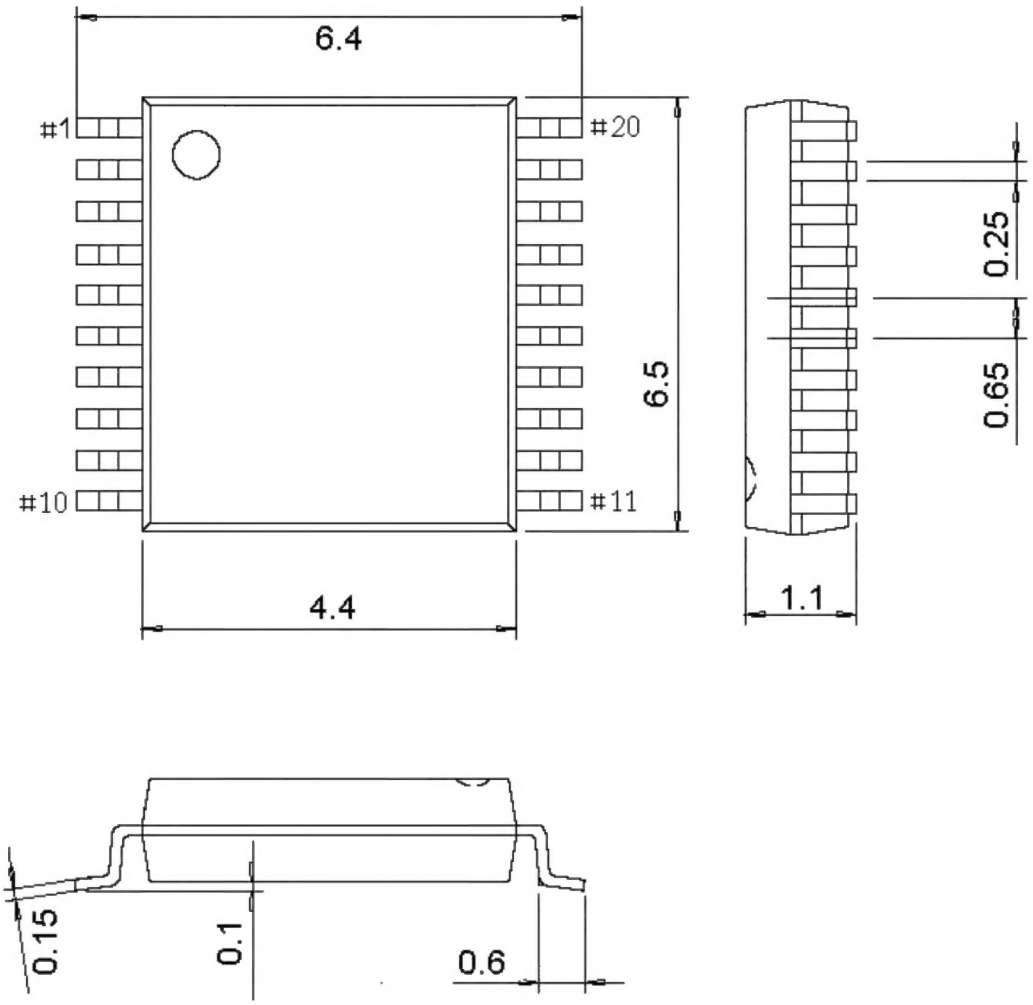
19.5 Other Parameters

Test conditions: TA=25°C, VDD12=4.5V～5.5V or VDD12=VDD=3.0V～3.6V.

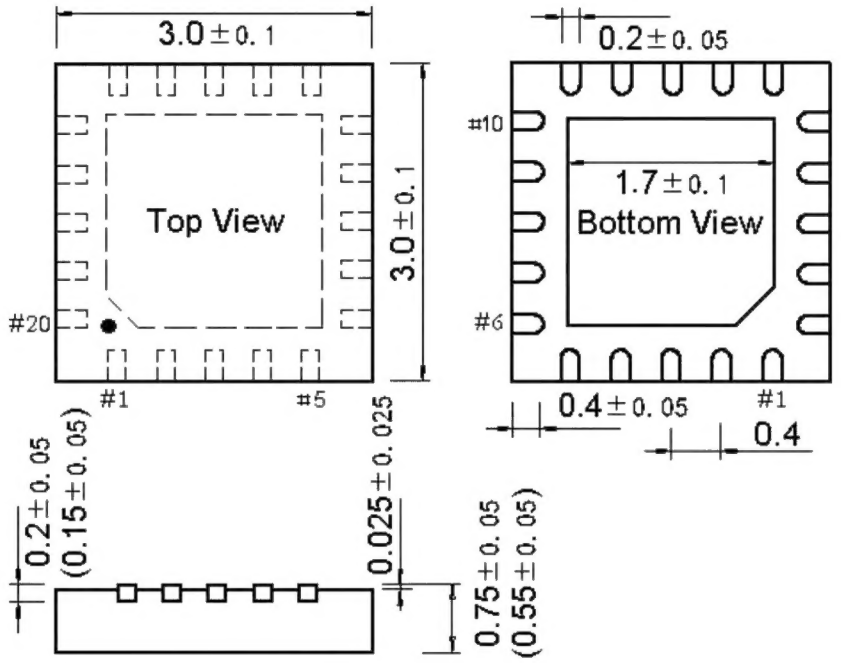
Symbol	Parameter description	Min.	Typ.	Max.	Unit
TERPG	Time to perform single erase/ program operation on Flash-ROM/EEPROM	2	5	8	mS
NEPCE	Flash-ROM/EEPROM erase/program cycle endurance	10K	Sampling value 100K		times
TDR	Data retention capability of Flash-ROM/EEPROM	10			years
VESD	ESD voltage on I/O pins	4K	Sampling value 8K		V

20. Package Information

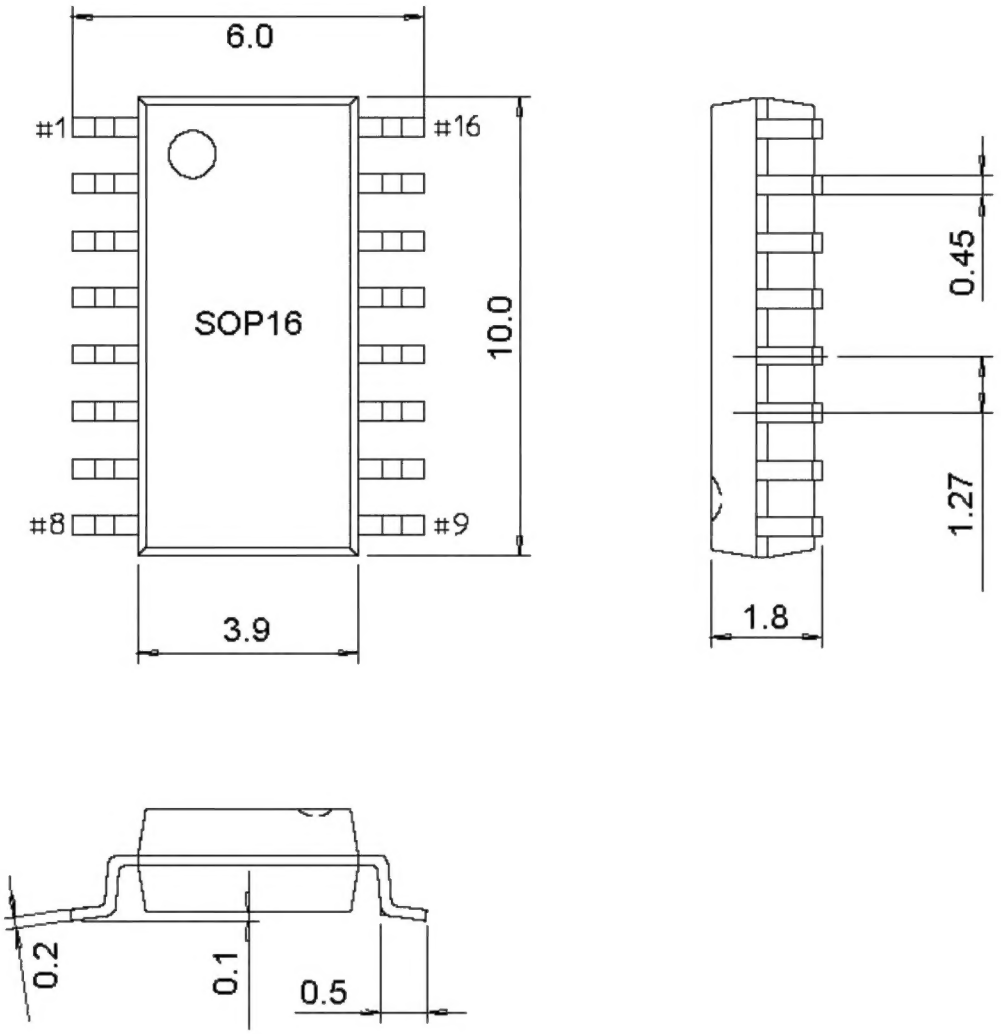
20.1 TSSOP20



20.2 QFN20-3*3



20.3 SOP16



21. Revision History

Revision	Date	Description
V0.99	October 28, 2020	Initial release
V1.0	December 25, 2021	Note that no external resistors are connected in series with USB pins. Description about bit reset optimized: Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.
V1.1	April 18, 2022	Description about ISINK deleted. Note that P1.0/P1.1 does not support full-width voltage output.
V1.2	April 26, 2022	Typos corrected: Description of PIN_FUNC in Section 10.3, and Touchkey calculation in Section 15.5.
V1.3	August 9, 2022	Correction of SOP16 pin 9#, 10# labeling errors, restore the relevant ISINK expression
V1.4	May 26, 2023	For new designs, only the CH543D and CH541T/G packages are retained, and the 48MHz main frequency is reserved for custom chips.
V1.5	September 12, 2023	Modified the recommended value of 7.1 power decoupling capacitors and refined 19 ambient temperatures